IPC Standards Activity

Vern Solberg
STC-Madison
vernsolberg@att.net

IPC Organization Background

- A Global Membership
  + 71% North America
  + 14% Europe
  + 13% Asia
  + 2% Rest of World

- Members: 3,076 representing 63 Countries
- 26 General Committees
- 250 Subcommittees and Task Groups
IPC Mission Statement

The IPC is a United States based trade association dedicated to furthering the competitive excellence and financial successes of its members world wide, who are participants in the electronic interconnection industry.

IPC Organization Structure

MEMBERS

Board of Directors

TAEC  EMSI Council  PWB Presidents Council  PWB Suppliers Council  Designers Council Executive Board  California Circuits Association Board  TMRC Steering Committee  AMRC Steering Committee

US!

SMEMA Council

Surface Mount Equipment Manufacturers Association
Standards Process

Task groups develop drafts of new standards and resolve comments at IPC meetings

There are four stages of standard development

1. Project Submission - TAEC approves form
2. Working Draft - gets project started
3. Proposal - solicits comments from industry
4. Interim Final - resolves comments from balloting

Standards Related to SMT Assembly Design and Process Implementation

- **IPC-A-610**, Acceptability of Electronic Assemblies
- **IPC-7095**, Design and Assembly Process Implementation for BGAs
- **IPC-7094**, Design and Assembly Process Implementation for Flip-Chip and Die Size Components
- **IPC-7093**, Design and Assembly Process Implementation for Bottom Termination Components
IPC-A-610E
Industry Standard for Acceptability of Electronic Assemblies

IPC-A-610 Document Scope-

- Visual quality acceptability requirements.
- Presents acceptance requirements for the manufacture of electrical and electronic assemblies.
Interpretation of Requirements

When the user elects to specify compliance with the mandatory requirements of this document:

Unless otherwise specified by the user, the word “shall”, signifies that the requirement is mandatory.

Deviation from any “shall”, requirement requires written acceptance by the user, e.g., via assembly drawing, specification or contract provision.

The words “should” and “may” reflect recommendations and guidance, respectively, and are used whenever it is intended to express non-mandatory provisions.

The Circuit Board Assembly is the Heart of Every Electronic Product

Source: Sharp
Defining Producability Levels

- Level A
  *General Design Complexity*

- Level B
  *Moderate Design Complexity*

- Level C
  *High Design Complexity*

Identifying Basic PCB Assembly Types

**IPC Type 1:**

*All devices attached to one side of circuit structure.*

**IPC Type 2:**

*Devices attached to both sides of circuit structure.*
Defining Assembly Classification

- **Class 1**
  - General Electronic Products
- **Class 2**
  - Dedicated Service Electronic Products
- **Class 3**
  - High Performance Electronic Products

*The Customer determines the class to which assembly is evaluated!*

Basic assembly definitions:

- **Primary side**
  - *side with highest component density*
- **Secondary side**
  - *side with lower component density*
- **Solder source side**
  - *surface exposed to wave solder*
- **Solder destination side**
  - *surface opposite wave solder*
SMT Assembly Assessment

Component-to-Land Alignment for Discrete Passive Components
**Maximum Side Overhang**

Acceptable-
Class 1, 2 - $\frac{1}{2} W$
Class 3 - $\frac{1}{4} W$

**End Overhang**

Rectangular End Termination Component

Reject – Class 1, 2, 3
Terminal end overhang not permitted for any class
Minimum Fillet Height

Acceptable-
Class 1- Evidence of wetting
Class 2, 3- $F = G + \frac{1}{4} H$

Lead Frame Packaged Semiconductors
Maximum Side Overhang

Gull Wing Lead

Acceptable:
- Class 1, 2 - $A = \frac{1}{2} W$
- Class 3 - $A = \frac{1}{4} W$

Maximum Toe Overhang

Toe overhang is permitted on gull wing lead devices but the overhang must not violate minimum design conductor spacing.

Acceptable – Class 1, 2, 3 if...
Minimum Fillet Height

Acceptable-
Class 1- Evidence of wetting
Class 2- \( F = G + \frac{1}{2} T \) *

Acceptable-
Class 3- \( F = G + T \) *

* In the case of a toe-down lead configuration, the minimum heel fillet height (F) shall extend at least to the midpoint of the outside bend radius.

Assessment of BGA Assembly
BGA Assembly
Accept / Reject Criteria

Typical Solder Defects:
- Solder bridging between contacts
- Opens, non wetted ball-to-board interface
- Excessive voiding in the solder ball contact
- Excessive voiding at the interface
  > Ball-to-board
  > Ball-to-package

Solder Ball Void Examples

Minimal Void
Void at Interface
Excessive Size
Void Over Via
Solder Bridge
Ball-to-Void Size Image Comparison for Common Ball Contact Diameters

<table>
<thead>
<tr>
<th>Solder Ball Diameter/ X-Ray Image</th>
<th>Void 0.20 mm Diameter</th>
<th>% Void Diameter</th>
<th>% Void Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.85 mm</td>
<td></td>
<td>24%</td>
<td>6%</td>
</tr>
<tr>
<td>0.75 mm</td>
<td></td>
<td>27%</td>
<td>7%</td>
</tr>
<tr>
<td>0.65 mm</td>
<td></td>
<td>31%</td>
<td>9%</td>
</tr>
<tr>
<td>0.55 mm</td>
<td></td>
<td>36%</td>
<td>13%</td>
</tr>
<tr>
<td>0.45 mm</td>
<td></td>
<td>44%</td>
<td>20%</td>
</tr>
<tr>
<td>0.40 mm</td>
<td></td>
<td>50%</td>
<td>25%</td>
</tr>
<tr>
<td>0.30 mm</td>
<td></td>
<td>67%</td>
<td>44%</td>
</tr>
</tbody>
</table>

Note: By prior agreement between supplier and customer, the maximum void area may be greater or less than the dimensions shown in Table.

Source: IPC-7095

Cause of Voiding

Trapped Flux-
*Reflow process does not allow enough time for flux to expel from the molten solder.*

Contamination-
*Contaminants from improperly cleaned printed circuit boards.*

Voiding can also be a carry over from voids already present in the solder ball during the package assembly process!
BGA Package Defect - Missing Solder Ball

Source: Glenbrook

Defect – Class 1,2,3

Solder Process Defects

Defect – Class 1,2,3
The document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology.

- The effect of BGA and FBGA on current technology and component types.
- Critical inspection, repair, and reliability issues associated with BGAs.

The intent is to provide useful and practical information to those who are using BGAs and those who are considering BGA implementation.
The BGA Implementation Document Includes:

1. BGA Component Selection Criteria  
2. Managing BGA Implementation  
3. Component Considerations  
4. PCBs and Other Mounting Structures  
5. Printed Circuit Assembly Design  
6. Assembly of BGAs on Circuit Boards  
7. Reliability  
8. Defect and Failure Analysis Case Studies

BGA Package Assembly Example

(Wire-Bond, Die Face-Up)

- Encapsulation
- Gold on Copper Bond Site
- Ball Contact
- Die Attach Material
- Silicone Die
- Substrate Interposer
PCB Design and Land Pattern Development

Example of solder joint between the ball contact and circuit board

Solder ball exhibits a uniform solder joint interface and is aligned symmetrically about the circuit board land pattern.

BGA Land Pattern Development

<table>
<thead>
<tr>
<th>Nominal Ball Diameter (mm)</th>
<th>Reduction</th>
<th>Nominal Land Diameter (mm)</th>
<th>Land Variation (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>25%</td>
<td>0.55</td>
<td>0.60 - 0.50</td>
</tr>
<tr>
<td>0.60</td>
<td>25%</td>
<td>0.45</td>
<td>0.50 - 0.40</td>
</tr>
<tr>
<td>0.50</td>
<td>20%</td>
<td>0.40</td>
<td>0.45 - 0.35</td>
</tr>
<tr>
<td>0.45</td>
<td>20%</td>
<td>0.35</td>
<td>0.40 - 0.30</td>
</tr>
<tr>
<td>0.40</td>
<td>20%</td>
<td>0.30</td>
<td>0.35 - 0.25</td>
</tr>
<tr>
<td>0.30</td>
<td>20%</td>
<td>0.25</td>
<td>0.25 - 0.20</td>
</tr>
</tbody>
</table>

Source: IPC-7095

The manufacturing allowance for land size is estimated at 0.1 mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC).
**BGA Solder Mask Clearance**

- **0.65 - 1.00 mm** contact pitch
  - Solder mask clearance: 0.07 mm (3 mils)

- **0.50** contact pitch
  - Solder mask clearance: 0.05 mm (2 mils)

**HD Circuit Routing for Fine-Pitch BGA**

- **Level 1**
  - 100 micron (4 mil) wide external ckt.
  - 75 micron (3 mil) wide internal ckt.
  - 275 micron (11 mil) dia. land pattern
  - 100 micron (4 mil) dia. filled blind via

- **Level 2**
  - 275 micron (7 mil) dia. stop pad

- **Level 3**
Planning for Automated Assembly

- BGA Component Placement and Clearances
  - An advantage of BGA packages over other high-pin count packages is the ability to be placed using existing surface mount placement equipment.
  - No special placement and clearance requirements are needed for the component pick and place operation, however, it is recommended that sufficient clearance (3 to 5 mm) be provided around BGAs when possible to facilitate inspection and rework.

Recommended IC Package Spacing for Edge Inspection
This document describes the design and assembly challenges for implementing Flip-Chip and Die-Size package technology and the effect of these devices on current technology.

The focus on the information is on critical inspection, repair, and reliability.

The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes.

The intent is to provide useful and practical information to those who are using Flip-Chip and Die-Size components and those who are considering their implementation.
A “wafer level” ball grid array (WLBGA) is a type of BGA where the body size is equal to the die size. All processing required to attach a silicon IC chip on a circuit board is done at the wafer level.

Comparing WLBGA contact pitch (e) to ball or bump contact diameter (b) range

<table>
<thead>
<tr>
<th>e</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.65</td>
<td>0.35</td>
<td>0.40</td>
<td>0.45</td>
</tr>
<tr>
<td>0.65</td>
<td>0.30</td>
<td>0.35</td>
<td>0.40</td>
</tr>
<tr>
<td>0.50</td>
<td>0.30</td>
<td>0.35</td>
<td>0.40</td>
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<tr>
<td>0.50</td>
<td>0.25</td>
<td>0.30</td>
<td>0.35</td>
</tr>
<tr>
<td>0.60</td>
<td>0.20</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>0.50</td>
<td>0.15</td>
<td>0.17</td>
<td>0.19</td>
</tr>
<tr>
<td>0.40</td>
<td>0.20</td>
<td>0.25</td>
<td>0.30</td>
</tr>
</tbody>
</table>
Die-Size BGA Packaging

- The JEDEC Standard 95-1 Section 7, Die Size (DSBGA) Design Guide standards defines the physical features of the finished device.
- Included are the bump and ball contact size and pitch variations, controlling tolerances for position and size.

JEDEC Standard contact pitch (e) and contact diameter (b) variations for DSBGA

<table>
<thead>
<tr>
<th>e = pitch</th>
<th>b min.</th>
<th>b nom.</th>
<th>b max</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.80 mm</td>
<td>0.40 mm</td>
<td>0.45 mm</td>
<td>0.50 mm</td>
</tr>
<tr>
<td>0.60 mm</td>
<td>0.35 mm</td>
<td>0.40 mm</td>
<td>0.45 mm</td>
</tr>
<tr>
<td>0.80 mm</td>
<td>0.25 mm</td>
<td>0.30 mm</td>
<td>0.35 mm</td>
</tr>
<tr>
<td>0.75 mm</td>
<td>0.40 mm</td>
<td>0.45 mm</td>
<td>0.50 mm</td>
</tr>
<tr>
<td>0.75 mm</td>
<td>0.25 mm</td>
<td>0.30 mm</td>
<td>0.35 mm</td>
</tr>
<tr>
<td>0.65 mm</td>
<td>0.35 mm</td>
<td>0.40 mm</td>
<td>0.45 mm</td>
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<tr>
<td>0.65 mm</td>
<td>0.25 mm</td>
<td>0.30 mm</td>
<td>0.35 mm</td>
</tr>
<tr>
<td>0.50 mm</td>
<td>0.25 mm</td>
<td>0.30 mm</td>
<td>0.35 mm</td>
</tr>
</tbody>
</table>
Document details key implementation issues:

• Design
  - Substrate Structure
  - PCB Design Requirements
  - Electrical Design
  - Thermal Design

• Requirements for Board Level Reliability
  - Materials and Processes
  - Design/performance/use
  - Environmental impact
  - Failure analysis

IPC 7093
Design and Assembly Process
Implementation for Bottom Terminal Components
This document describes the design and assembly challenges for implementing Bottom Termination surface mount Components (BTCs) whose external connections consist of metalized terminations that are an integral part of the component body.

Throughout this document the word “BTC” can mean all types and forms of bottom only termination components intended for surface-mounting.

This includes such industry descriptive nomenclature as QFN, DFN, SON, LGA, MLP, and MLF, which utilize surface to surface interconnections.

The focus of the information is on critical design, assembly, inspection, repair, and reliability issues associated with BTCs.

Common BTC Configurations

Discrete devices

- SON
- QFN
- Laminate Based QFN
- Laminate Based LGA
QFN Packaging

Because of their small outline and low cost the QFN is of high interest to industry.

Perimeter input/output pads are located on the outside edges of the package.

The center section surface is retained for die attach and thermal transfer.

QFN Package Assembly

Die are attached to the lead-frame array using a thermally conductive compound followed by conventional wire bond processing.

Following wire-bond operations the multiple unit assembly is typically incased in a mold compound prior to singulation and electrical test.
Design and Assembly Process Considerations for QFN Type BTC Packages

- Most QFN components have a uniform contact size and pitch.
- Some of the BTC packages, however, may require very wide pads for power and ground pins.
  - Non uniform contact geometry can result in both shorts and opens due to board warping, package warping, insufficient or excessive solder paste.

Contact Pitch and Terminal Dimensions

- A majority of the no-lead products have been supplied with either 0.65mm or 0.50mm pitch but, devices with 0.40mm pitch are also being offered for limited applications.

<table>
<thead>
<tr>
<th>Contact Pitch (e)</th>
<th>Dimension (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>b</td>
</tr>
<tr>
<td>0.65</td>
<td>min. 0.35 nom. 0.40 max. 0.45</td>
</tr>
<tr>
<td>0.50</td>
<td>min. 0.25 nom. 0.30 max. 0.35</td>
</tr>
<tr>
<td>0.50 ¹</td>
<td>min. 0.20 nom. 0.25 max. 0.30</td>
</tr>
<tr>
<td>0.40</td>
<td>min. 0.15 nom. 0.20 max. 0.25</td>
</tr>
</tbody>
</table>

¹ Optional variation to expand the clearance between terminal features
The IPC-7093 standard recommends that to optimize the reliability of the solder joints on the perimeter lands, the standoff dimension after reflow processing should be approximately 50 microns (2 mils).

Many users believe that this thickness will provide clearance for cleaning and furnish a robust electrical and mechanical interface.

To achieve this standoff dimension the thickness of solder paste printed onto the lands should be no less than 100 microns (4 mils).

When solder is to be used for joining the thermal features it is recommended that, rather than one large opening matching the DAP outline, a pattern of smaller openings be furnished on the thermal pad region to provide approximately 50% to 80% printed solder paste coverage.
Using a Partitioned Print Pattern

By partitioning the print pattern on the thermal pad, solder paste will retain a more planer profile during reflow soldering.

*Rather than coagulating in the center of the thermal pad during reflow soldering, the partitioned solder pattern will maintain a uniform interface between surfaces.*

Concerns...

- For a majority of commercial applications the no-lead package is finding wide acceptance.
- There remains, however, a number of concerns by users developing products for use in harsh environments.
  - This is due in part to the very low stand-off height of the no-lead package and the electronic industries transition to RoHS compliant solder alloys and PCB materials.
Standards should...

- Show the relationship to DFM and DFA
- Minimize time to market
- Contain simple or simplified language
- Include only specified information
- Focus on end product performance

Include a feedback system on use and problem solving for future improvement.

Standards should not...

- Inhibit Innovation
- Increase time to market
- Restrict competition
- Increase cycle time
- Define how a product is made

Contain any requirement that cannot be defended with data

Thank you