Evolving Industry Standards: Design and Assembly Process Implementation for Embedding Passive and Active Components

An Introduction to IPC-7092

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Introduction

• Printed circuits have traditionally served as the platform for mounting and interconnecting active and passive components on the outer surfaces.
  – Companies attempting to improve functionality and minimize space are now embedding a broad range of components within the circuit structure.
  – Both uncased active and passive component elements are candidates for embedding.
  – The decision to embed components within the multilayer circuit structure, however, must be made early in the design process.
Substrate Interposer Application

Example source: IPC International Technology Roadmap
Drivers for Embedding Components

- Smaller board for same functions
- Enable higher component density
- Improve performance
  - shorter circuit paths
  - Expanding bandwidth
  - Increasing signal speed
  - Minimizing noise
- Reducing total assembly costs
• Topics of discussion-
  – Evolution in embedded component standards
    • Overview of current and evolving standards
  – Selection criteria for embedding components
    • Embedded component structure variations
  – Embedding passive components
    • Formed and discrete device attachment
  – Embedding active components
    • Attachment and interface methodology
  – Semiconductor package development
    • Embedding single and multiple die elements
Evolution in Embedded Component Standards
Overview of current and evolving standards

- **IPC-2316** *Design Guide for Embedded Passive Device Printed Boards*
- **IPC-4811** *Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards*
- **IPC-4821** *Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards*
- **IPC-4101** *Specification for Base Materials for Rigid and Multilayer Printed Boards*
- **IPC-6012** *Qualification and Performance Specification for Rigid Printed Boards*
IPC-7092: Design and Assembly Process Implementation for Embedded Components

• SCOPE
  – This document describes the design and assembly challenges for implementing passive and active components, in either formed or inserted methodology, into a printed board
  – The completed structure including internal electronic components is ready for surface mount and/or through-hole component attachment
  – The multilayered structure becomes a complete product ready for further processing in an assembly process and be made from organic, inorganic (ceramic) or both types of material
IPC-7092 cont.

• Purpose
  – The target audiences for this document are managers, design and process engineers, and technicians who develop electronic assemblies that include an embedded component printed board as a part of the product.
  – The purpose is to provide useful and practical information to those who are involved in the decision making of either formed or inserted, passive or active components and to help establish inspection techniques, testing processes, and reliability validations.
IPC-7092 Cont.

- This document, although not a complete recipe, identifies many of the characteristics that influence the successful implementation of a robust embedded component process.

- In many applications, the variation between forming and inserting methods and materials are reviewed with the intent to highlight significant differences that relate to the decision as to when, why, or how to establish the quality and reliability of the final product.

- The information also establishes the robustness that the embedded portion of the product can survive the continued processing in order to complete an Embedded Component Printed Board Assembly.
Embedded PCB Planning

• The first decision that must be made is whether or not to adopt an embedded component solution.
• Depending on the application, cost, performance, or some other metric may influence the decision.
• Several factors must be considered:
  – Value range of passive components selected for embedding (formed or inserted)
  – Availability of discrete passive components suitable for inserting
  – Procurement of bare ‘tested’ die prepared for embedding
Formed Passive Components

• Formed resistors-
  – Several companies have developed material sets and fabrication processes for thick-film resistors, requiring only a conventional screen-printing process

• Formed capacitors-
  – The capacitor dielectric separating the copper surfaces of the power and ground plane an organic polymer thick film or ceramic thin film composite.

• Formed inductors-
  – A specific inductance can be developed using thin circuit trace patterns configured in spiral like geometry
Inserted Passive Components

• As an alternative to forming component parts, many companies are inserting discrete passive components within the multilayer circuit.

• Inserted resistors elements-
  – The smallest discrete resistor is furnished in a standard 01005 package outline in all standard values

• Inserted capacitors-
  – The capacitor family includes the 01005 package outline as well, but value range will be limited

• Inserted inductors-
  – Small outline inductors are available from limited sources with values ranging up to 100nH
Selecting Resistors for Embedding

% Distribution by Resistor Value

Data source: iNEMI
Selecting Formed Capacitor Materials

Formed capacitor materials can be organized in two categories: laminates or pastes/inks.

Source: IPC-2316
• Some of the influencing factors are:
  – Available tolerance of the embedded parts and aging behavior
  – Drift limits following thermal shock or humidity exposure
  – Temperature coefficient impact on capacitance or resistance
  – Power handling capacity, breakdown field and leakage currents
  – Parts that will need circuit tuning or active trimming
  – Special requirements e.g., low noise metal film resistors
  – Available space for embedded parts, especially large capacitor values
  – Density of embedded parts – the cost effectiveness of embedding components may be maximized at some intermediate component density
• Perhaps the more difficult question to answer is “Which embedding methodology will be used—formed passive or inserted discrete passive devices or a combination of both?”

• The most common approach is to perform an economic analysis of embedded passive components—
  – Estimate the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the production panel
  – Determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new panel yield computed
  – Define the available manufactured components intended for insertion or the materials required for producing formed passive components
Selecting Components for Embedding

- Select passive components closely coupled to active device
- Formed passive devices will have broad tolerance range
- Inserted passive device values enable closer tolerances
- All embedded components will require a unique identifier [1]

[1] To enable material control the designer will identify embedded component elements with a unique reference designator that is related to a specific layer of EPCB structure.
EPCB Cost Analysis for Passive Components

- The analysis focuses on differences in system cost between embedded passive and discrete passive solutions and assembly costs associated with non-embeddable parts.
Defining EPCB Structure Groups

- The IPC-7092 document furnishes common EPCB structure groups-
  - The grouping is intended to identify some of the precision and control needed in the manufacturing processes.
  - The component handling, positioning, and attachment method are determined based on the manufacturers’ capability and the completed base-core’s ability to withstand multiple processing procedures and exposures.
<table>
<thead>
<tr>
<th>Type</th>
<th>Config</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1</td>
<td>Passive chip components “inserted” on one side of a mounting base</td>
<td>Applications include developing a base-core ready for additional layers</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Active semiconductor chip components “inserted” on one side of a mounting base</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Passive chip and active semiconductor chip components “inserted” on one side of a mounting base</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>Passive chip components “inserted” on both sides of a mounting base</td>
<td>Applications include developing a base-core ready for additional layers or component mounting</td>
</tr>
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<td></td>
<td>2</td>
<td>Active semiconductor chip components “inserted” on both sides of a mounting base</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Passive chip and active semiconductor chip components “inserted” on both sides of a mounting base</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>Passive chip components “inserted” on one side of a mounting base with formed components within the base</td>
<td>Applications include developing a base-core ready for additional layers or component mounting or a completed electronic assembly</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Active semiconductor chip components “inserted” on one side of a mounting base with formed components within the base</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Passive chip and active semiconductor chip components “inserted” on one side of a mounting base with formed components within the base</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>Passive chip components “inserted” on both sides of a mounting base with formed components within the base</td>
<td>Applications include developing a base-core ready for additional layers or component mounting or a completed electronic assembly</td>
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<tr>
<td></td>
<td>2</td>
<td>Active semiconductor chip components “inserted” on both sides of a mounting base with formed components within the base</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Passive chip and active semiconductor chip components “inserted” on both sides of a mounting base with formed components within the base</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>Passive formed components within a base-core intended for further layering</td>
<td>Applications include base-core ready for additional layer and/or component mounting or both</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Passive formed components within a base-core intended for component mounting</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Passive formed components within a base-core intended for further layering and component mounting</td>
<td></td>
</tr>
</tbody>
</table>

Source: IPC-7092
Type A

A1 Base-core example with inserted passive components on one side

A2 Base-core example with inserted active components on one side

A3 Base-core example with inserted passive and active components on one side

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

Example source: IPC-7092
Type B

**B1 Base-core example with inserted passive components on two sides**

**B2 Base-core example with inserted active components on both sides**

**B3 Base-core example with inserted passive and active components on both sides**

1. Copper clad (2 side) core; 2. Component mounting base; 3. Cavity modified prepreg; 4. Copper clad dielectric

Example source: IPC-7092
Type C

C1 Base-core example with formed passive components in the mounting base and inserted passive components on one side

C2 Base-core example with formed passive components in the mounting base and inserted active components on one side

C3 Base-core example with formed passive components in the mounting base and inserted passive and active components on one side

1-Copper clad (2 side) core; 2- Component mounting base; 3-Cavity modified prepreg; 4-Copper clad dielectric

Example source: IPC-7092
Type D

**D1** Base-core example with formed passive components in the mounting base and inserted passive components on both sides

**D2** Base-core example with formed passive components in the mounting base and inserted active components on both sides

**D3** Base-core example with formed passive components in the mounting base and inserted passive and active components on both sides

1-Copper clad (2 side) core; 2- Component mounting base; 3- Cavity modified prepreg; 4- Copper clad dielectric

Example source: IPC-7092
Type E

**E1** Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides

**E2** Mounting base example with formed passive components inside the mounting base turning the product into a base-core

**Figure 7-21** E3 Mounting base example with formed passive components inside the mounting base plus additional layering added to one or both sides

1-Copper clad (2 side) core; 2-Copper clad dielectric

Example source: IPC-7092
Structure Type F1
Embedded Core Technology

- The process description for the F1 embedded core structure is based on a ‘face down’ semiconductor element mounting and laser ablated and plated via interface technology.

Type F1 is a combination of HDI micro via and ultra-fine line process based on a modified semi-additive Cu plating technology and precise component assembly methodology.
Structure Type F1
Embedded Core Technology

• The process begins with laser marking fiducial targets on the surface of an ultra-thin copper foil base layer.

• A pattern of adhesive material that is slightly larger than the semiconductor outline is printed onto the copper surface and partially cured to furnish a stable surface for device attachment.

• Using the fiducial target features on the copper surface as a guide, the component(s) are placed into the partially cured adhesive pattern with the Cu plated terminal features facing down.

• A thermal curing process follows to complete the bonding of the semiconductor element to the copper foil base.
AT&S ‘Chip First’ Process Sequence

Die element w/ Cu plated terminals

Die attach adhesive

CEM backed copper foil

Heated die placed onto adhesive pattern and snap cured

Copper clad prepreg laminated over die element-CEM backing removed

Core section completed using conventional HDI and laser via interconnect
Planning EPCB Fabrication Process Flow

C3 Base-core example with formed passive components in the mounting base and inserted passive and active components on one side

Example source: IPC-7092
EPCB Base Material Selection

• Industry roadmaps consistently point to materials and process refinement as the key enablers for improving product performance and manufacturing efficiency.

• Likewise, the conversion to lead-free solder technologies has forced the laminate industry to make significant refinement to all packaging and substrate related materials.

• The substrate methodologies being used for embedded semiconductor and passive component packaging will likely utilize one of the following dielectric systems:
  – FR-4 or FR-5 Epoxy/Glass  —— Primary PCB base material
  – BT Epoxy/Glass  —— Semiconductor substrate mtl.
  – Polyimide film (PI)  —— Used for harsh environments
Base Material Attributes

• Although many material systems can furnish excellent functional capability they do not all have a broad supply base.

<table>
<thead>
<tr>
<th>Type</th>
<th>Resin</th>
<th>Reinforcement</th>
<th>$T_g$ (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR-4</td>
<td>Epoxy</td>
<td>Woven E Glass</td>
<td>130-170+</td>
</tr>
<tr>
<td>B-T</td>
<td>Bismaleimide triazine/epoxy</td>
<td>Woven E Glass</td>
<td>170-230</td>
</tr>
<tr>
<td>PI</td>
<td>Polyimide</td>
<td>Woven E Glass</td>
<td>250-265</td>
</tr>
</tbody>
</table>

Data source: IPC-4101

Because BT and PI may have more limited applications, fabrication costs are somewhat higher than the more common FR-4 based substrate.
Formed Resistor Process Variations

- Materials incorporated into the circuit board during manufacture:
  - Become part of the PCB structure or substrate
  - Can be formed on PCBs internal layers or on the PCBs outer surface.

- Common forms –
  - Thick film (paste/liquid)
  - Thin-film (sheet form)

Photo source Ticer
### Formed Resistor Material / Supplier Variations

<table>
<thead>
<tr>
<th>Application</th>
<th>Material type</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Screen print</td>
<td>Polymer thick film</td>
<td>Acheson</td>
</tr>
<tr>
<td>Screen print</td>
<td>Polymer thick film</td>
<td>Asahi</td>
</tr>
<tr>
<td>Screen print</td>
<td>Polymer thick film</td>
<td>Electra</td>
</tr>
<tr>
<td>Screen print</td>
<td>Polymer thick film</td>
<td>Metech</td>
</tr>
<tr>
<td>Screen print</td>
<td>Polymer thick film</td>
<td>MIE</td>
</tr>
<tr>
<td>Thin-Film Ceramic(^1)</td>
<td>Sheet form</td>
<td>DuPont</td>
</tr>
<tr>
<td>Thin-Film (NiCr)(^1)</td>
<td>Sheet form</td>
<td>Ticer</td>
</tr>
<tr>
<td>Thin-Film (NiP)(^1)</td>
<td>Sheet form</td>
<td>Omega Industries</td>
</tr>
<tr>
<td>Thin-Film (Pt)(^1)</td>
<td>Sheet form</td>
<td>Dow</td>
</tr>
</tbody>
</table>

\(^1\) Requires lithographic imaging and etching process
Thick Film Resistor Forming Process

• Polymer thick-film (PTF) resistors can be printed directly onto the laminate surface.
• The application of these materials require only conventional screen print processing to provide the resistor pattern.
  – The paste-like PTF material is available in resistance values that range between 1 ohm and 1 meg ohm per square while the CTF materials value will range between 10 ohms and 10K ohms.

*Example source: Manncorp*
Resistor Printing Process

• Screen printing is typically adopted for applying resistive paste or ink patterns---
  • Photo sensitive emulsion is applied onto the screen surface, photo-imaged and developed to provide the resistor pattern.

• Screen print processes do have a number of variables-
  – Screen material stretch or shrinkage
  – Emulsion exposure variation
  – Affects of screen cleaning process

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Thick Film Resistor Issues and Concerns

- Resistance ranges and process variations
- Expectation for resistor value stability
- Affect of environment conditions -
  - Thermal stability
  - Moisture
  - Time (age affect)
- Material adhesion
- Laser trim accessibility
- Suitable coatings for protecting element
Design Criteria for Sheet Film Resistor Elements

• The resistive foil is an integrated part of the system and should not be considered as an isolated element when designing the EPCB.

• Factors that effect system performance are:
  
  • Circuit configuration
  • Circuit thickness and material type
  • Thermal conductivity of the dielectric
  • Proximity to power or ground planes
  • Ambient operating temperature range
  • System cooling or heat sinking
  • Resistor size (total resistor area)

Example source: Ohmega Technologies
Foil Based Thin-Film Resistor Material

- Thin-film NiCr \(^{[1]}\) or NiCrAlSi \(^{[2]}\) is sputter coated onto Cu foil sheet stock-
  - Furnished in 25, 50, 100 and 250 ohms/square sheet resistivity
  - Basic sheet resistor tolerance is +/- 5% but, laser trimming can be used to improve resistor tolerance

\[ \text{[1] NiCr: Nickel-Chromium} \]
\[ \text{[2] NiCrAlSi: Nickel-Chromium-Aluminum-Silicon} \]
Thin-Film Deposition Process

Argon Filled Vacuum Chamber

Copper foil

Surface atoms ejected from target

Magnetic field

Argon ions accelerated to target

Magnetron Sputtering Cathode

Target

Target backing plate

Magnets

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Thin-Film Resistor Forming Process

• Resistor elements are formed using a two step chemical etch process
  – Compensation must be made for etching process tolerance

• Finished resistor tolerance in the range of +/- 8% to +/- 10%
  – Laser trimming can be used to improve resistor tolerance

*Minimum recommended feature size is 0.25mm*
Thin-Film Resistor Forming Process cont.

1. NiCr sputter coated onto Cu foil sheet
2. Image and chem etch resistor pattern
3. Laminate w/element pattern face-down, image circuit on Cu
4. Chem etch to form land pattern and circuit
Calculating Formed Resistor Element Value
Ohms per Square

\[ R = \frac{pL}{A} \]

- \( R \) = resistance in ohms
- \( p \) = resistivity

Resistivity (\( p \)) a material property constant at a given temperature expressed in resistance units (ohms) for area and length expressed in \( \Omega/\square \)
- resistance varies by the L/W aspect ratio

Example: \( L \) (2.0mm) x \( W \) (1.0mm) = 2 sq
Where thickness is constant, \( R \) will be constant for each square area.
Basic Value Planning for Formed ‘Bar’ Resistors

The value of the bar resistor element (thick-film or Thin-film) is determined by the basic value of the paste, ink or sheet composition and the number of square segments between land pattern features.

<table>
<thead>
<tr>
<th>Resist material</th>
<th>Copper land</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 sq = 1KΩ</td>
<td>2 sq = 2KΩ</td>
</tr>
<tr>
<td>2 1/2 sq = 2.5KΩ</td>
<td></td>
</tr>
</tbody>
</table>
Serpentine Resistor Element Planning

• A serpentine resistor can be designed as a bar resistor with the exception of the corner squares (right-angle bends).

• Due to the change in current density at right-angle path, the effective number of the corner square is 0.56.

Example:
Sheet resistance (RS) = 100 Ω
No. of squares = 37
No. of corner squares = 16

Total No. of effective squares = 37 + (16 @ 0.56) = 45.9 Ω 46
Resistance value = 46 x 100 = 4.6 KΩ

Data and example source: Ohmega Technologies
General Formed Resistor Layout Guidelines

• Establish optimum base value for resistors-
  – Refer to material suppliers dimension guide for details.

• Determine min/max resistor feature sizes needed-
  – Recommend maintaining basic rectangular shapes.
  – Printed patterns should be greater than 0.30mm wide.

• Allow 125μm spacing between copper features for test probe access and laser trim.
Formed Capacitors

- There are two techniques commonly adopted for embedded capacitor forming:
  - Dielectric material deposited directly onto a Cu foil or the circuit layers using a thick-film screening process.
  - Dielectric layer laminated between opposing copper circuit layers.
Formed Capacitor Material / Process Variations

- Process variations-
  - Etched copper planes on two sides of a filled or unfilled dielectric layer (Planar)
  - Printed or photo-imaged
    - Polymer thick film
    - Ceramic thick film
    - Ceramic filled polymer
- Monetary impact-
  - Minimal for all photo-print products
  - Precision screen-printing may be required
  - Precision photo-imaging commonly required
  - Some material may need high temperature curing
Formed Inductors

- Formed inductors are current loops configured in the Cu foil to induce a magnetic field for short term storing and controlling inductive energy.

Example source: IPC-2316
Formed Inductor Design

– The inductance is determined by the length of the spiral and number of turns.
– The spacing between turns will control the resonant frequency of the inductor.
– A wider spacing will typically reduce capacitance and raise the inductance frequency.
Inserted Passive Devices

• Resistors
  – Small outline, thin profile
  – Broad value range, wide tolerance choice

• Capacitors
  – Small outline, varying profile
  – Limited value range and tolerance

• Inductors
  – Small outline, varying profile
  – Very limited value range
SMT Resistor Use History

1206 0805 0603 0402 0201 01005

01005

- Precision surface mount resistor with 1% tolerance have been designed to meet the continuing demand for thinner, smaller outline devices.

- The 01005 device measures only 0.40mm x 0.20mm x 0.15mm — This is 55% smaller than the 0201 chip resistor.

Example source: KOA-Speer
Capacitor Sourcing

• A number of companies are supplying small outline capacitors with a thickness of 0.15mm-0.20mm for the 01005 type component and 0.20mm-0.30mm for the 0201.

• The 01005 and 0201 type capacitors with a C0G dielectric, for example, are available in a value range between 5.0pf and 100pf.

• The X7R dielectric capacitors, on the other hand have a value range 68pF to 470pF for the 01005 type and 68pF to 10,000pF for the 0201 size component.

• A very thin (0.15mm) capacitor family, although available from some sources, have a limited value range.
Capacitor Value Range Limitations

The discrete SMT capacitor family includes the 01005 and 0201 outline capacitors as well but the dielectric type, working voltage and value range for the smaller device outlines may be somewhat limited from traditional sources.

Example source: Murata Mfg.
Thin-Film Capacitors

These devices are available with capacitance values from 0.8 to 1000 pF

- High reliability silicon oxide–nitride dielectric
- Low loss—typically 0.04 dB in a 50 W system
- Operation through 26 GHz
- Wide temperature operation

Nom. Thickness- 0.13mm
Outline dim.- 1mm to 1.7mm sq.
( depending on value)
Sourcing Discrete Inductor Components

- There are basically only two types of inductor types that are suitable for embedding into the PCB-
  - multilayer ceramic
  - Thin-film multilayer

- The multilayer ceramic products have a relatively small outline but their thickness is too great.

- The thin-film inductor provides a small outline and a moderately thin profile more compatible for embedding.
Ceramic Multilayer Inductor

- Although the basic 0402 device outline may be acceptable, the 0.5mm profile thickness will be far too great for most embedded applications.

Source: KOA Spear
Multilayer Thin-Film Inductor

- Excellent for high frequency applications
- Low DC resistance and high Q
- Suitable for reflow and wave soldering
- Low tolerance ±2% available

Source: KOA Spear
Component Termination Variations

- Interconnection can be made using deposited solder paste and reflow processing or secured using an anisotropic conductive polymer and a thermal cure process.

- Miniature passive components mounted onto the inner layer base substrate will require placement systems with a high level of positional accuracy.
Alternative Termination Process

• Rather than relying on solder or conductive polymer for electrical interface, passive devices can be mounted onto the substrates surface with a non-conductive adhesive

• Electrical termination can then be made directly onto the component terminals with micro-via ablation and copper plating process

To achieve the most reliable micro-via to component interface the user should specify copper plated terminals when ordering passive components.
Embedding Active Components

• Progress in developing high density embedded component substrate capability has accelerated through the cooperation and joint development programs between a number of government, industry and technical universities.

• In addition to these joint development programs, several independent laboratories and package assembly service providers have developed a number of proprietary processes for specific applications.
Semiconductor Die Quality Classification

<table>
<thead>
<tr>
<th>Quality Level</th>
<th>Visual Inspection</th>
<th>Electrical Characteristics</th>
<th>Early Failures</th>
<th>Long Term Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 1 Known Good Die</td>
<td>Sampling specified on product spec.</td>
<td>All test items Assured $^1$</td>
<td>Detection Assured</td>
<td>Assured</td>
</tr>
<tr>
<td>Level 2 Known Tested Die</td>
<td>Sampling specified on product spec.</td>
<td>All test items Assured $^1$</td>
<td>Not Assured</td>
<td>Not Assured</td>
</tr>
<tr>
<td>Level 3 Probed Die</td>
<td>Sampling specified on product spec.</td>
<td>Some tests Skipped $^2$</td>
<td>Not assured</td>
<td>Not assured</td>
</tr>
</tbody>
</table>

$^1$Corresponding to the specified criteria for packaged products

$^2$The same criteria level as packaged products with burn-in

- It is strongly recommended that the embedded die candidate be at least a ‘Level 2’ before use.

Source: IPC-7092
Semiconductor Interface Preparation

- Mounting the semiconductor (face-up or face-down) will require additional metallization processing while in the wafer format:
  - The aluminum bond sites must be over-plated with Cu
  - A Cu redistribution layer (RDL) will be required for die elements having less than 100μm bond pitch

Example source: Semiconductor Design
Terminal Face-Down Assembly

- Develop substrate with cavity feature to accommodate component thickness
- Place component onto prepared land pattern features
- Cure or reflow attachment material, clean, apply underfill and cure
- Laminate cap layer to complete component encapsulation
Terminal Face-Up Assembly

- Develop substrate with cavity feature to accommodate component thickness
- Place component face-up onto prepared Cu pattern features.
- Cure attachment material and laminate cap layer to complete component encapsulation.
- Ablate vias at terminal sites and Cu plate to complete interface with upper layer circuit.
Via-to-Semiconductor Interface

Example source: ASE Global
SMT/BGA EPCB Assembly Sequence

- Surface mount assembly follows the sequential build-up and electrical test of the EPCB structure-
  - Print solder paste onto land patterns on top surface
  - Place components onto lands, reflow solder, clean
  - Print tacky flux on array pattern on lower side of EPCB
  - Place alloy spheres onto flux, reflow solder, clean, test
BGA/Microelectronic Assembly Sequence

- Microelectronic assembly follows the sequential build-up and electrical test of the basic EPCB structure -
  - Apply die attach film to top surface of structure
  - Place die element and perform wire-bond process
  - Encase wire-bonded die element with mold compound
  - Print tacky flux on array pattern on lower side of EPCB
  - Place alloy spheres onto flux, reflow solder, clean, test
### Economic Factors

#### Positive factors:

<table>
<thead>
<tr>
<th>Increase</th>
<th>Decrease</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of printed boards fabricated on a panel due to decreased board size.</td>
<td>Printed board area can be smaller due to a reduction in the number of surface mounted passive components.</td>
</tr>
<tr>
<td>Surface mounted component density resulting in shorter coupling between devices.</td>
<td>Wiring density simplified due to the integration of resistors and bypass capacitors within the substrate.</td>
</tr>
<tr>
<td>Potential for higher second level assembly process yields</td>
<td>Reduction in overall assembly costs, solder process defects and rework</td>
</tr>
</tbody>
</table>
Economic Factors cont.

**Negative factors**

<table>
<thead>
<tr>
<th>Increase</th>
<th>Decrease</th>
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<tbody>
<tr>
<td>Greater printed board cost per unit area due to greater fabrication process complexity.</td>
<td>Printed board fabrication throughput may be impacted by process variables.</td>
</tr>
<tr>
<td>Higher wiring density requirements due to the reduced printed board area.</td>
<td>Lower printed board fabrication yield due to process related defects.</td>
</tr>
</tbody>
</table>
Summary and Conclusion

• Several PCB suppliers with experience in build-up circuits are already heavily involved in embedding both passive and active components
• Although ‘formed’ resistor and capacitor processes are very mature, a number of users are not satisfied with their physical stability and wide tolerance range
• With the availability of smaller and thinner passive device outlines from a wide supply base, many companies recognize the practical advantage for embedding discrete passive elements
  – Less restrictive value selection
  – Wide resistor and capacitor value range
  – Very good tolerance stability
• Embedding the semiconductor element is where many companies may find a significant roadblock—
  – Procurement of semiconductors in a wafer format
  – Outsourcing wafer metallization and thinning
  – How to test, what to test and features needed to enable testing
• Ideally, the originating companies will bring together the two primary suppliers; the circuit board fabrication specialist and the assembly service provider
  – These partnerships must be willing to adjust their portion of the generated revenue against the overall process yield (sharing of losses from PCB fabrication process defects as well as damaged components)
IPC-7092
Design and Assembly Process Implementation for Embedded Components

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Thank you