Package on Package (PoP) Applications, Requirements, Infrastructure and Technologies

SMTA OR Chapter
March 16, 2011

Lee Smith
VP Marketing & Biz Development
Amkor Technology Inc.
Lee.Smith@amkor.com
Outline

Background: Application Trends & Requirements for Package Stacking
- Mobile Handset Requirements Drive to PoP
- 1st Generation PoP Development / Deployment Summary
- PoP Infrastructure

1st Generation PoP Technologies
- Warpage considerations
- PoP – SMT, and BLR considerations
- Trends / Requirements for higher density PoP

Next Generation PoP Technology
- PoP with TMV® (Thru Mold Via) Interconnects
- TMV technology benefits
- TMV PoP surface mount / brd level reliability studies
Application Specific Packaging
Optimize for Size, Integration, Cost / Performance

Driven by the need for more I/Os and high performance

1970s 1980s 1990s 2000s
DIP SOP LCC QFP PGA TQFP / FQFP BGA SiP FBGA / CSP

DLP®
Application Specific Packaging Optimize for Size, Integration, Cost / Performance

Driven by the need for small size and low cost

1970s 1980s 1990s 2000s
DIP SOP LCC QFP PGA TQFP / FQFP BGA SiP FBGA / CSP

SSOP / TSOP 3D Pkg QFN WLCSP

Package-on-Package PoP

Stacked Die CSP

DLP courtesy of Texas Instruments  TouchChip courtesy of UPEK

© 2011 Amkor Technology, Inc. March 2011, SMTA OR LSMIT
Amkor New Package Intro History
(OEM collaboration for apps specifics / infrastructure)
Market Demands Put Added Pressures on Consumer Electronics Manufacturers

Source: Mario Bolanos “Packaging Trends Applied Research Opptys at U. of Binghampton CAMM
Smartphone Advancements would not have been possible without 3D Pkg and PoP technologies

3D packaging address integration challenges to enable semiconductor advancements . . .

. . . to deliver physical world benefits
And 3D Is Back As the Dimensions of Design, Manufacturing and Mobile Content Converge

It’s an MP3 player and ...

It’s an e-mail terminal and ...

It’s a camera and ...

... an MP3 player, e-mail terminal, phone, camera, TV, radio, compass, game machine

It’s a game machine and ...

It’s a compass and ...

It’s a TV and ...

It’s a radio and ...

© 2004 Gartner, Inc. and/or its Affiliates. All Rights Reserved.
3D Pkg Development – Collaboration!

- 1\textsuperscript{st} Generation 3D (Die Stacking)
  - Memory IDMs for wirebond combo memory (MCP) were 1\textsuperscript{st}.
    - Followed by outsource or development collaboration w/ SATS.
  - Logic + memory stacking, IDM collaboration with SATS followed by IDM internalization for dual source, Fabless collaboration with SATS.

- 2\textsuperscript{nd} Generation 3D (Package Stacking or PoP)
  - Nokia collaboration with Amkor drove technology platform development.
  - OEM / IDMs collaboration with Amkor for PoP product development / deployment.
  - Next Gen PoP (TMV\textregistered) Amkor driving – multiple areas of collaboration.

- 3\textsuperscript{rd} Generation 3DIC w/ TSV
  - Full supply chain collaboration.
Die vs. Package Stack Analysis

(Business model’s huge impact on Cost of Ownership)

3D SiP
(Dominant for Combo Memory & Digital + analog)

Vertical Die Qty 2 3 4 5

Cumulative Die Yield High Low
Die / Test Costs Low High
Require burn-in No Yes
Die/Memory Sourcing Simple Complex
Sourcing flexibility No Yes
Design flexibility No Yes

PoP
(Dominant for multi-media Apps proc + complex memory stacking)
Amkor 3D Collaboration – Technical Papers

• Amkor / Nokia – PoP Joint Industry Tech Papers
  – ECTC 2002 Extremely thin BGA / CSP and BLR (etCSP)
  – ECTC 2003 Package stack thin CSP and BLR (PSetCSP)
  – ECTC 2007 High Density PoP Stacking and BLR (PoP w/ SoP)
  – EMPC 2009 Mechanical qualification of TMV® PoP w/ ST Micro

• Joint Industry Papers on PoP, SCSP and TMV®
  – ECTC 2006 PoP Stacking Study vs Warpage – w/ Sharp & Panasonic
  – IMAPS DPC 2006 PoP Stacking & BLR Study – w/ Spansion & Panasonic
  – SMTAI 2008 TMV PoP Stacking & BLR Study – w/ Sony Ericsson
  – IMAPS DPC 2009 High density 8 die stack – w/ Intel
  – SMTAI 2009 TMV PoP Stacking App Notes & BLR – w/ Celestica
**1st Generation PoP Development**

**PSvfBGA Core Technologies from CSP Tool Box**

- Thin die (4~3mil, 1mil D/A) (from SCSP)
- Low loop wire (from SCSP)
- Pin gate mold (from etCSP)
- Package stacking application notes
- Pb free material set (from SCSP)

**Advantages**
- Low wire sweep
- Low mold void
- Can place the lands around encapsulation area
- Thin molding
1st Generation PoP – Infrastructure Development

**OEMs**
- Architecture stacking
- 12 major OEMs in Handset and DSC market adopting PoP

**Industry Standards**
- JEDEC – JC.11.2 Design guide, JC11.11 POD, JC-63 pin outs

**Equipment**
- Panasonic, Siemens, Fuji, Unovis, Assembléon, Hitachi

**EMS / ODM**
- 5 major EMS providers in production or development

**Logic IDM**
- 15 major IDMs adopted PoP

**Memory IDM**
- 8 major Memory suppliers adopted PoP

**Amkor**
- Full service – Develop, Design, Model, Standards, bottom, top PoP, Modules, pre-stacked engineering samples, BLR

Practical Components – stocks Amkor 12 and 14mm bottom / top DC samples
- [www.amkor.com](http://www.amkor.com) Design, stacking, test and Brd level reliability (joint study papers)
Bottom PoP (PSvfBGA) Sizing criteria

- Wire count?
- Wiring Density
- Number of i/o to top package?
- Number of i/o to motherboard? (bottom side)
- Die size?
# 1st Gen. PoP Design Guidelines (Wire bond)

- 0.65mm top / 0.5mm bottom -

<table>
<thead>
<tr>
<th>Body Size</th>
<th>Package Interconnect Matrix</th>
<th>Ball Count</th>
<th>Bottom Side Ball Count</th>
<th>Die Size</th>
<th>Wire Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>15</td>
<td>104</td>
<td>- 300</td>
<td>&lt; 5.5</td>
<td>- 320</td>
</tr>
<tr>
<td>11</td>
<td>16</td>
<td>112</td>
<td>- 350</td>
<td>&lt; 6.0</td>
<td>- 360</td>
</tr>
<tr>
<td>12</td>
<td>18</td>
<td>128</td>
<td>- 400</td>
<td>&lt; 7.5</td>
<td>- 420</td>
</tr>
<tr>
<td>13</td>
<td>19</td>
<td>136</td>
<td>- 450</td>
<td>&lt; 8.0</td>
<td>- 460</td>
</tr>
<tr>
<td>14</td>
<td>21</td>
<td>152</td>
<td>- 550</td>
<td>&lt; 9.0</td>
<td>- 520</td>
</tr>
<tr>
<td>15</td>
<td>22</td>
<td>160</td>
<td>- 700</td>
<td>&lt; 10.0</td>
<td>- 560</td>
</tr>
</tbody>
</table>

PSvfBGA, PoP bottom package

General guideline based on advanced substrate design rule

For higher I/O count requirements apply 0.4mm ball pitch on bottom
Multiple variations of pitch and ball size have been successfully paired to accommodate various mold cap or bare FC die heights.

Target value for standoff f2 will influence stacking yield and will depend on:

- Warpage characteristics of the top and bottom packages
- The stacking capability and process of the end assembly house.
JEDEC PoP Standards

- **JC-11 (Design and Mechanical Outlines)**
  - PoP Design Guide covers top and bottom packages to ensure mechanical integrity.

**JEDEC PUBLICATION 95**

**DESIGN GUIDE 4.22**

Fine-pitch, Square Ball Grid Array Package (FBGA) Package-on-Package (PoP)

- **JC-63 (MCP task group defines memory Pin-outs)**
  - PoP 10 to 16mm body sizes approved
  - 0.65 to 0.4mm pitch memory interfaces
Figure 3.12.2-4
Ball Outline – 128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

Source: JEDEC
1st Gen. PoP w/ FC Bare Die

- **0.50mm Pitch on Top Side** (unit : mm)

<table>
<thead>
<tr>
<th>Body Size</th>
<th>Package Interconnect</th>
<th>Die Size</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Matrix</td>
<td>Ball Count</td>
<td>w/o Dam</td>
</tr>
<tr>
<td>10</td>
<td>19</td>
<td>136</td>
<td>&lt; 5.40</td>
</tr>
<tr>
<td>11</td>
<td>21</td>
<td>152</td>
<td>&lt; 6.40</td>
</tr>
<tr>
<td>12</td>
<td>23</td>
<td>168</td>
<td>&lt; 7.40</td>
</tr>
<tr>
<td>13</td>
<td>25</td>
<td>184</td>
<td>&lt; 8.40</td>
</tr>
<tr>
<td>14</td>
<td>27</td>
<td>200</td>
<td>&lt; 9.40</td>
</tr>
<tr>
<td>15</td>
<td>29</td>
<td>216</td>
<td>&lt; 10.40</td>
</tr>
</tbody>
</table>

Note: Values subject to change without notice.

---

**Package size**

**Max die size**

**PoP Ball pads**

**SM Dam to prevent resin bleed**

**Package interconnect pad**
Mobile Phones Finish 2010 Strong
Smartphones Drive Growth & PoP Demand

<table>
<thead>
<tr>
<th></th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>CAGR '10-'15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semi TAM ($B)</td>
<td>42.7</td>
<td>39.5</td>
<td>49.1</td>
<td>55.8</td>
<td>60.0</td>
<td>61.8</td>
<td>65.6</td>
<td>70.8</td>
<td>7.6%</td>
</tr>
<tr>
<td>Yr/Yr Growth</td>
<td>-8.0%</td>
<td>-7.5%</td>
<td>24.3%</td>
<td>13.6%</td>
<td>7.6%</td>
<td>2.9%</td>
<td>6.2%</td>
<td>8.0%</td>
<td></td>
</tr>
</tbody>
</table>

Source: Gartner
PoP Warpage, SMT & BLR considerations
PSvfBGA Warpage Considerations

Structural CTE Mismatch

Bottom Package

Shrinks less

Shrinks more

Cool down

25°C

expands less

expands more

Heat up

260°C
Design Factors Impacting Warpage

- **Die**
  - Die size
  - Die Thickness

- **Mold**
  - Material property
  - Shrinkage
  - Thickness

- **Die attach**
  - Material property
  - Thickness

- **Laminate Substrate**
  - Properties
  - Thickness
  - Cu ratio
  - Routing
JEDEC Standard Warpage Legend and Example Data

+ Cry

- Smile

<table>
<thead>
<tr>
<th>Temp</th>
<th>Sample 1</th>
<th>Sample 2</th>
<th>Sample 3</th>
<th>Sample 4</th>
<th>Sample 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°C</td>
<td>30</td>
<td>37</td>
<td>41</td>
<td>30</td>
<td>37</td>
</tr>
<tr>
<td>75°C</td>
<td>-36</td>
<td>-47</td>
<td>-32</td>
<td>-40</td>
<td>-30</td>
</tr>
<tr>
<td>125°C</td>
<td>-45</td>
<td>-37</td>
<td>-33</td>
<td>-45</td>
<td>-34</td>
</tr>
<tr>
<td>175°C</td>
<td>-70</td>
<td>-65</td>
<td>-54</td>
<td>-68</td>
<td>-59</td>
</tr>
<tr>
<td>225°C</td>
<td>-92</td>
<td>-88</td>
<td>-81</td>
<td>-92</td>
<td>-87</td>
</tr>
<tr>
<td>260°C</td>
<td>-79</td>
<td>-74</td>
<td>-76</td>
<td>-72</td>
<td>-71</td>
</tr>
<tr>
<td>225°C</td>
<td>-92</td>
<td>-88</td>
<td>-81</td>
<td>-92</td>
<td>-87</td>
</tr>
<tr>
<td>175°C</td>
<td>-70</td>
<td>-65</td>
<td>-54</td>
<td>-68</td>
<td>-59</td>
</tr>
<tr>
<td>125°C</td>
<td>-45</td>
<td>-37</td>
<td>-33</td>
<td>-45</td>
<td>-34</td>
</tr>
<tr>
<td>75°C</td>
<td>-32</td>
<td>-40</td>
<td>-30</td>
<td>-36</td>
<td>-47</td>
</tr>
<tr>
<td>25°C</td>
<td>52</td>
<td>73</td>
<td>73</td>
<td>64</td>
<td>66</td>
</tr>
</tbody>
</table>
Recommendations for improving SMT and Stacking yield

- **Warpage data processing methods**
  - A: Package corner to package corner
  - B: Array corner to array corner
  - C: Inner and outer corners of ball matrix (diagonal)
  - D: Ball matrix corner to corner (sides)

- **Appropriate methods**

<table>
<thead>
<tr>
<th>Top Pkg</th>
<th>Bot Pkg</th>
<th>Use Methods</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>C &amp; D</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Use Methods</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B*, C &amp; D</td>
</tr>
</tbody>
</table>

* Method B to check for interference of warped packages at the center
PoP Stacking SMT Lines Options

One time reflow

Pre-stacking

Source: Panasonic Factory Solutions and Nokia – KGD Workshop Sept 2006
## Dipping Flux and Paste Property

<table>
<thead>
<tr>
<th>Item</th>
<th>Dipping flux</th>
<th>Dipping paste (new)</th>
<th>Screen printing paste (ref)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viscosity (Pa.s)</td>
<td>20</td>
<td>30</td>
<td>200</td>
</tr>
<tr>
<td>Thixotropic Index</td>
<td>0.4</td>
<td>0.8</td>
<td>0.6</td>
</tr>
<tr>
<td>Powder size (um)</td>
<td>---</td>
<td>5 – 25</td>
<td>30</td>
</tr>
<tr>
<td>Flux content (%)</td>
<td>---</td>
<td>20</td>
<td>11</td>
</tr>
<tr>
<td>Reflow condition</td>
<td>Air</td>
<td>Air</td>
<td>Air</td>
</tr>
</tbody>
</table>

Dipping paste solder (new) showed improved transcription

Screen paste solder (ref)
Transcription Material - Paste vs. Flux

Solder paste transcription

Solder paste keep connecting the solder ball with the land \(\rightarrow\) good joints

Flux transcription

With large warpage, the solder ball cannot touch down on the land during reflow \(\rightarrow\) open joints
# 14mm PoP Pb-Free BLR Study IMAPS DPC 2007 w/ Spansion

<table>
<thead>
<tr>
<th>Leg #</th>
<th>Pad finish of Top Package</th>
<th>Solder ball Top pkg</th>
<th>Pad finish of bottom package</th>
<th>Solder ball Bottom pkg</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leg 1</td>
<td>NiAu</td>
<td>SAC405</td>
<td>NiAu</td>
<td>SAC305</td>
<td>N/A</td>
</tr>
<tr>
<td>Leg 2</td>
<td>NiAu</td>
<td>SAC405</td>
<td>CuOSP</td>
<td>SAC305</td>
<td>N/A</td>
</tr>
<tr>
<td>Leg 3</td>
<td>NiAu</td>
<td>SAC405</td>
<td>CuOSP</td>
<td>SAC305</td>
<td>Multiple reflow passes by Panasonic to simulate prestack</td>
</tr>
<tr>
<td>Leg 4</td>
<td>NiAu</td>
<td>SAC405</td>
<td>NiAu</td>
<td>SAC305</td>
<td></td>
</tr>
<tr>
<td>Leg 5</td>
<td>NiAu</td>
<td>SAC405</td>
<td>CuOSP</td>
<td>LFA3</td>
<td></td>
</tr>
</tbody>
</table>

* In all cases CuOSP finish JEDEC Drop Boards used
Leg 1 showed the worst performance as predicted
- NiAu pad on bottom BGA – IMC crack

Cu OSP finish on bottom BGA improves life by 2.6X
- Legs 2, 3 & 4

Alternate Ni doped solder ball alloy greatly improves drop reliability
- Leg 5 – No failures, robust IMC layers

Failure Interface same on all legs
- Bottom side of bottom package

Failure Criteria
- Any intermittent discontinuity of resistance greater than 1,000 ohms lasting for 1 microsecond or longer. The first event of intermittent discontinuity followed by 3 additional such events 5 subsequent drops
ECTC 2007 Amkor Study for PoP 2nd Level Underfill

- 14 x 14mm PoP
- 0.65mm 152 top
- 0.5mm 353 bottom

Full DOE Matrix
- UF Patterns
- Reworkable
- Non reworkable

Control
(Non-Underfill)

Full Underfill

Corner Dot

Corner L
Next Generation PoP Requirements and Solution
Next Gen PoP: Increased - Integration, Miniaturization, Performance & Collaboration

Signal processing
- µP integration Bband + applications - increased pin counts
- µP core speed 2 – 3X w/ each node (1GHz @ 45nm)
- Transition to FC accelerates from 65nm

Memory Interface
- Higher speed memory interface SDRAM – DDR -> LP DDR2
- Wider memory bus 16 – 32
- Shared to split bus to (2 channel) architectures

Increased pin counts with size reduction requires 0.4mm pitch top and bottom
Warpage control with thinner / higher density PoP stacks
Signal integrity optimization, decoupling cap integration
Power efficiency and thermal mgmt
Si / pkg co-design for PoP to optimize for cost / performance

<table>
<thead>
<tr>
<th>Device Dynamics</th>
<th>2008</th>
<th>2010</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor I/O</td>
<td>400</td>
<td>600</td>
<td>800</td>
</tr>
<tr>
<td>CMOS Node</td>
<td>65nm</td>
<td>45nm</td>
<td>28nm</td>
</tr>
<tr>
<td>Peak Power</td>
<td>400mW</td>
<td>800mW</td>
<td>1.2 W</td>
</tr>
<tr>
<td>Ave. Die Size</td>
<td>64mm²</td>
<td>50mm²</td>
<td>50mm²</td>
</tr>
</tbody>
</table>

© 2011 Amkor Technology, Inc. Amkor restricted release to SMTA March 2011, SMTA OR LSMIT
1st Gen PoP Technologies limit PoP I/O and Bottom Stacked Die Density – Requiring New Technology

- Die stacking in bottom package requires thicker mold cap
- New memory architectures require higher I/O interfaces
- Higher Semiconductor density requires package size reduction
- Thin form factors and increased battery size require thinner PoP stacks
- Improved warpage control required when go thinner with higher density

- A new bottom PoP technology is needed to continue growth
Thru Mold Via Technology (TMV®)

- Enabling technology for next generation PoP reqmts
  - Improves warpage control and PoP thickness reduction
  - TMV removes bottlenecks for fine pitch memory interfaces
  - Increases die to package size ratio (30%)
  - Improves fine pitch board level reliability
  - Supports Wirebond, FC, stacked die and passive integration

14 x 14mm 6 net daisy chain next generation PoP test vehicle
- 0.4mm thick mold cap with molded underfill encasing
  - 7 x 7mm Flip Chip daisy chain die at 220µm bump pitch
  - 32 tiny 01005 size 0 ohm resistors (to represent decoupling caps)

Top View
200 Solder Lands
@ 0.5mm pitch
memory interface

TMV™
14 mm 620 / 200

Bottom View
620 BGAs @
0.4mm pitch

TMV test vehicle reported at ECTC 2008
Joint tech paper at SMTAI August 2008
What is TMV® (Thru Mold Via) Technology?

• TMV is an ablation method to allow solderable connections thru a mold cap.

• TMV applies to wirebond, stacked die, flip chip devices (both area array solder and fine pitch CuPillar) and packages with discrete components embedded. TMV could also be applied to FlipStack® (combo FC+WB) and FC w/ TSV stacks.
TMV® Memory Interface Scaling Benefit

- Size reduction through memory interface pitch reduction
- Baseline design: 7x7mm die, 200 I/O top package IF, 2 row perimeter
TMV PoP Warpage Improvement
14mm 620 Package Warpage Comparison

Source: SMTAI 2008 Paper w/ Sony Ericsson
TMV® Interface Pitch Considerations

- **0.5mm TMV pitch**
  - 12mm 168 2 row In HVM with 0.35mm mold cap (2+0 wirebond stack)
  - 14mm 240 3 row In HVM with 0.28mm mold cap (single die FC die)

- **0.4mm TMV pitch**
  - In HVM with 0.25mm mold cap (single die FC)

- **TMV solder ball size and hole size is selected for SMT yield while avoiding solder bridging**
Media Tablets, 1Q11 Update: The Next Killer Application (increased 3D Density)

- iPad 2 & rival prices and time-to-maturity leaves Apple ahead of competitors
- Operating systems morphing into ecosystem plays
- OS and hardware evolution will make Media Tablets a more viable PC alternative in some cases
- Consumer enthusiasm for alternative mobile devices leading to strong uptake of media tablets
- Will slow mobile PC adoption in mature markets as households forgo additional mobile PC buys
- Even in the professional market, media tablets are being considered, delaying some PC replacements.

Source: Gartner
### TMV® PoP Design Guidelines

- 0.40mm top / 0.4mm bottom -

<table>
<thead>
<tr>
<th>A</th>
<th>B (Package Interconnect, 2 row)</th>
<th>C</th>
<th>D*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Body Size</td>
<td>Matrix</td>
<td>Ball count</td>
</tr>
<tr>
<td>10</td>
<td>23</td>
<td>168</td>
<td>529</td>
</tr>
<tr>
<td>11</td>
<td>26</td>
<td>192</td>
<td>676</td>
</tr>
<tr>
<td>12</td>
<td>28</td>
<td>208</td>
<td>784</td>
</tr>
<tr>
<td>12</td>
<td>29</td>
<td>216</td>
<td>841</td>
</tr>
<tr>
<td>13</td>
<td>31</td>
<td>232</td>
<td>961</td>
</tr>
</tbody>
</table>

**Notes:**
- **Package Size (A)**
- **Max. die size (D)**
- **Footprint-top (B)**
- **Footprint-bottom (C)**
- **0.25-0.40mm**

**Illustration only for TMV WB type**
TMV® PoP chip cap assy from SMTAI 2008 joint paper

01005 resistor:
400 * 200 * 130 um (X * Y * Z)

Screen printing

Chip mounting

Reflow

TMV substrate after SMT < FC attach  SMT process

Note: 01005 resistors are thinner than caps

© 2011 Amkor Technology, Inc.  Amkor restricted release to SMTA  March 2011, SMTA OR LSMIT
TMV® PoP SMT Summary

- Single pass reflow enables optimum logistics

- Surface mount trials at Amkor with 12x12mm 168 ball 0.5mm pitch PoP interface (ref. slide 8), using following parameters resulted in 100% yield (about 25K units, 20 lots)
  - SMT stacking material (flux) : Senju 529D-1
  - Flux volume : 250um dip depth
  - SMT Equipment : Assembleon D9
  - Bake condition prior to SMT : 125°C 8HR N2 condition

- Process studies required for different flux or paste material and dip depth
**TMV®PoP First Pass SMT Yield – Amkor Trials**

<table>
<thead>
<tr>
<th>Body (A)</th>
<th>Foot print – top (B)</th>
<th>Foot print – bottom (C)</th>
<th>Bot Pkg Die Size</th>
<th>Top Pkg Die Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>12x12mm</td>
<td>0.50mm pitch 168 pad 2 row</td>
<td>0.5mm pitch 401 I/O</td>
<td>6.2x6.5x0.075mm</td>
<td>9.0x5.0x0.1mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.0x4.7x0.075mm</td>
<td>8.0x7.5x0.08mm</td>
</tr>
</tbody>
</table>

- Dippable flux: Senju Deltalux 529D-1
- Air reflow, 242C Peak
- Sample size: 47 lots, ~50K units

Reference: IMAPS DPC 2010
Recommendations for improving TMV® PoP SMT Stacking yield

• Reflow
  – Reflow peak temperature: 235 – 245°C, Time above Liquidus: 45 – 75 sec
  – Avoid long soak time at flux activation temperature, excessive soak time results in flux burn off/dry off causing Head-in-Pillow joints for top to bottom package interconnects:
  – Recommendation: Choose flux with recommended pre-heat time of 60 to 75°C between 150 – 180°C

• Additional Recommendations
  – Process development on flux or paste material and dip depth
  – Increasing top package ball size to compensate for excessive warpage of top package
TMV® PoP Board Level Reliability Studies

• **Package and Board Details**

<table>
<thead>
<tr>
<th>Body (A)</th>
<th>Foot print – top (R)</th>
<th>Foot print – bottom (R)</th>
<th>Bot Pkg Die Size</th>
<th>Top Pkg Die Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>12x12mm</td>
<td>0.5mm pitch 168 pad 2 row</td>
<td>0.5mm pitch 401 I/O</td>
<td>6.2x6.5x0.075mm 4.0x4.7x0.075mm</td>
<td>9.0x5.0x0.1mm 8.0x7.5x0.08mm</td>
</tr>
</tbody>
</table>

  – Via sizes for Bottom Package: Small and Large
  – Board Thickness: 1.0mm
  – Board Pad size: 0.28mm NSMD

• **Board Level Temperature Cycling**

  – -40<>125C, 2 cycles per hour
  – 5000+ cycles completed, NO FAILURE

• **Board Level Drop Test (Nokia Condition)**

<table>
<thead>
<tr>
<th>Critical Locations</th>
<th>Small Via</th>
<th>Large Via</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st failure</td>
<td>72</td>
<td>70</td>
</tr>
<tr>
<td>Mean life</td>
<td>147.4</td>
<td>205.3</td>
</tr>
<tr>
<td>Characteristic life</td>
<td>160.9</td>
<td>230.9</td>
</tr>
<tr>
<td>Slope</td>
<td>4.815</td>
<td>2.676</td>
</tr>
</tbody>
</table>
TMV® PoP Board Level Reliability Results

- **Drop Data (Failures in Bottom package to board interconnects only)**
  - Bottom packages with Small or Large TMVs exceed reliability requirements of no failures in 30 drops at 5% failure rate
  - Reliability improves with No Connect corner balls

**Functional corner joints**
1st failure @ 70 drops

**No Connect corner joints.**
1st Failure @ 92 drops

---

\( \beta_1 = 4.8147, \eta_1 = 160.8986, \rho = 0.9946 \)

\( \beta_2 = 2.6758, \eta_2 = 230.8885, \rho = 0.9888 \)

\( \beta_1 = 5.0442, \eta_1 = 187.9451, \rho = 0.9658 \)

\( \beta_2 = 2.8816, \eta_2 = 303.3530, \rho = 0.9904 \)
Summary

- ~ 325 million PoP components shipped in 2010 up from < 5 million in 2005. Forecasted to grow at same high rate as Smartphones
- DDR2 2 channel and other new memory architectures driving higher density PoP memory interfaces
- Amkor pioneered 1st Generation PoP (PSvfBGA) and now leading in Next Gen high density PoP with TMV® technology shipping in HVM
- One pass SMT PoP stacking enables optimization of supply / logistics and lowest total cost of ownership
- Amkor and Universal Instruments planning 14mm 620 / 200 TMV PoP SMT stacking study and industry report to facilitate SMT yield / quality optimization