Designing for Advanced Surface Mount Assembly

Jay Gorajia
Director, Consulting Manufacturing Services

Agenda

- Introduction
- Standards
- Specific Issues
- The Business Case

Resolving manufacturability issues earlier... so they don’t cost you time and money
Introduction (why we are here)

- The explosive growth of high-density packaging has created a tremendous impact on the electronics assembly and manufacturing industry.

- Ball Grid Array (BGA), Chip Scale Packaging (CSP), Direct Chip Attach (DCA), chip-on-board (COB), and system-in-package (SiP), and flip-chip technologies are taking the lead in advanced manufacturing processes.
Cramming more in

IC Packages - Enable density and performance improvements

Designing with the Assembler in mind

You want us to assemble that!
### ARE THERE ANY STANDARDS

Designing with the Assembler in mind...

- **IPC 7351B** – footprint standards
  - Supersedes IPC-SM-782A
- **IPC AJ-820A** - Assembly and Joining Handbook
- **IPC C 406** - Design and Application Guidelines for Surface Mount Connectors
- **IPC CI 408** - Design and Application Guidelines for the Use of Solderless Surface Mount Connectors
- **IPC D 279** - Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies
Design Methodologies of High Density Interconnects

- **IPC/JPCA-2315**, Design Guide for High-density Interconnect Structures and Microvias
- **IPC-2226**, Sectional Design Standard for High-density Interconnect (HDI) Printed Boards
- **IPC/JPCA-4104**, Qualification and Performance Specification for Dielectric Materials for High-density Interconnect Structures (HDI)
- **IPC-6016**, Qualification and Performance Specification for High-density Interconnect (HDI) Structures
Goals of Assembly Manufacturer

- Prevent defects earlier instead of reacting to them later
- Introduce products to market faster
- Ensure the highest product quality and reliability
- Reduce costs at every design/production phase
- Ensure customer contract requirements are met
- Ensure continual customer satisfaction
- Enable continuous process improvement
- Streamline product cycle from design - manufacturing

Assembly Risks

- Risks with the BOM or AVL?
- Risks with component placement?
- Risks with adequate solderability?
- Risks with good joint creation?
- Risks to Testability?
- Will I be able to rework it, if needed?
Risks with the BOM or AVL

- **BOM + AVL Validation**
  - Identify alternate supplier form and fit issues
  - Specify the tolerances for like components
  - Includes height comparison
  - System identifies parts outside of your specifications

---

Risks with adequate connectivity (joint)

Accurate placement and pin to pad matching is critical for BGA component assembly
Risks with component placement

- Tall components too close to rout or Conveyed Edge can be damaged.
- Component to Component spacing varies by component types and orientation.

Risks with adequate solderability

- Heel & Toe Solder Joints
- Left & Right Solder Joints

- Pin to pad mismatch is the #1 reason for unreliable solder joints.
Risks with adequate solderability

- Tombstoming

Traces under low-lying components can cause the component to rock, causing a poor solder joint.

Risks with Rework and Placement

All Component to Component spacing based on all possible bodies combined.
Risks to Testability

- Testpoint analysis

Testpoints cannot be covered by components

Will I be able to rework it, if needed

- Component spacing surrounding BGA and complex packages
Additional design considerations

- Netlist Analysis
  - Catches fatal issues – opens and shorts
  - Confirm Gerbers and CAD netlists match

Additional design considerations

- HDI
  - Soldermask missing clearance for via will cause vias to fill with solder mask
  - Pad crosses drill
THE BUSINESS CASE

Business Pressures in Design

<table>
<thead>
<tr>
<th>Top Business Pressures Driving Improvements in PCB Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Need to launch products quickly</td>
</tr>
<tr>
<td>Demand for lower cost products</td>
</tr>
<tr>
<td>Demand for higher quality products</td>
</tr>
<tr>
<td>Reduced development budgets</td>
</tr>
</tbody>
</table>

DFM addresses four of these pressures

Aberdeen Group, Why Printed Circuit Boards Matter to the Executive, February, 2010
Oh the Pain!

What pains are you feeling today?

- Recently had a design scrapped in manufacturing
- Not meeting product release schedules
- Taking too many revision spins per design
- New product introductions are over budget
- Have to maintain larger staff than necessary to manage issues
- Have to get product back to customer and stuck with rework load
  - Yield issues

The cost of design change

Source: Aberdeen Group, 2006, 2011; DARPA, 2006; MIT, 1999
Causes for Fabrication Hold

Courtesy of P. D. Circuits, Hampstead, NH
Data collected over six months, 2008

DFM could have prevented 66.7% of the holds

26% of jobs put on hold
Value Proposition

- Valor DFM users average 57% fewer revision spins than non-Valor users
- The average savings in material costs alone equates to $20,800 per design

Aberdeen Research, Printed Circuit Design Integrity, May, 2007

DFM Categories

<table>
<thead>
<tr>
<th>Number of DFM Categories Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fabrication</td>
</tr>
<tr>
<td>Assembly</td>
</tr>
<tr>
<td>HDI</td>
</tr>
<tr>
<td>Microvia</td>
</tr>
</tbody>
</table>

Plus:
- Netlist Validation
- BOM Validation
- Approved Vendor List (AVL) Validation

766 Total Checks
Value Proposition

- Fewer revision spins per design
- Fewer major production issues
- Significant time savings in release schedule

Valor NPI

Resolving manufacturability issues early... so they don’t cost you time and money

Synchronized with Your Supply Chain

- Same analysis as your suppliers use
- Same rules settings to know their process capabilities
- Same data format streamlines the Design-to-Manufacturing flow
- Modifications done by fabricator can be analyzed to validate correctness
Questions?

Thank You!

Jay Gorajia
Jay_Gorajia@mentor.com