Introduction

- Technology is evolving.
- Miniaturization, New designs, Pad geometry, Components, New solder alloys and new board plating and finishes will arise,
- The pace of shrinking geometries is inescapable.
- So will be the defects.
- Fine pitch BGAs, CSPs, flip-chips and wafer-level packaging for high-value assemblies will demand more fine-scale finesse in detection, discrimination and control.
Auto Electronics: How many PCBs?
The drivers of the electronics industry have changed

Source: Prismark Partners – August 2012
Factors to Consider

- Factors that affect PCB Assembly yields could be classified into several main categories including:
  - Assembly Materials
  - **PCBs and Components**
  - Process Methods resulting Joint Quality

- Printed Circuit Board (PCB) or PWB fabrication is one critical aspect of the electronics manufacturing that **often is a grey area** for most SMT / Wave assembly Engineers

- PCB quality has a direct impact on Solderability, Productivity & Reliability.

- Most often SMT / Wave / Manual Soldering techniques are also a grey area for PCB Fabricator / Engineers
The Gap

As Number of defects and flaws detected at PCB Assembly is mostly due to:

• Lack of Experience in Design for Assembly (DfA)

• Lack of assembly manufacturing knowledge,

• No firm grip on Assembly processes (SMT Reflow, Wave, Selective, Robotic & manual soldering)

• Lack of understanding on assembly equipment – Printer/Placement/Reflow
Objective

This presentation is to bridge this gap & to realize potential cost benefits by:

- Enlightening on Bare Board (PCB) related issues seen at Assemblers
- Understanding their impact on Quality, Through-put, Reliability – Overall COST of Assembly
- Simple Solutions to overcome those defects at no extra cost in PCB Fabrication
- Improving your share of business at Customers
Design for Manufacturability

If important criteria are overlooked in the design stage, there is little an assembler can do later to compensate for the problems created.
Why DFM?

• Lower development cost
• Shorter development time
• Faster manufacturing start of build
• Lower assembly and test costs
• Higher quality
Commonly Observed Issues in the Field... (OEMs & EMS)

Impact on the overall solder joint reliability:

- Legend Printing / Via Hole Fill / Tenting
- Rework @ Legend Printing
- Pad definition versus Solder mask definition.
- Solder mask Printing Accuracy
- Surface Finish
- Effect of Thermal relief for Hole-Fill
- Board thickness & Others issues
IPC/NPL PCB Problems Survey 2012

- Electrical Shorts/Opens: 27.30%
- Solder Mask: 5.30%
- Cosmetic Faults: 14.70%
- Via Hole Failure: 8.00%
- Delamination: 6.00%
- Finish Solderability: 38.70%

Bob Willis Jan 2012
Micro BGA Open Issue
Set Top Box Manufacturer
Via Hole Tenting & White Legend

Richard Puthota
Alpha India
Aug 2012
The image is of a OSP PCB, under micro BGA Package where, a few solder pads have not caught the solder paste. Rework involving 100% removal of micro BGA & re-solder.
Please have a close look at the combination effect of:

a) solder mask coating thickness +

b) Via hole fill (as in previous slide) with solder mask protruding like a volcano +

c) legend marking white ink on top of via fill
BGA Spheres Inspected for oxidation on their surface, Co-planarity may not be an issue as it is a micro BGA
PCB Visual Inspection at U5 location

1. Each PCB in the multiple array has few variables unique to each other.

2. When micro BGA device sits on this pad, it could experience a non-coplanar surface due to the height created by RHS bottom side via-hole solder mask fillet and the white legend ink lump.

3. Solder mask alignment is off. The effect could be paste coming on to mask which can experience high surface tension.

4. Some vi-holes partially filled and few not filled also. (Gasket effect)
Huge solder mask off-set. Imagine if paste is printed over this and component is placed. Recipe for disaster!!!

Can see dual coating of solder mask.
Solder paste Print quality – Good!
CVP-390 SACX0307 Plus
PCB Visual Inspection at U5 location

- Via hole-fill not co-planar.
- Usually colourless resin is used for fill and scrubbed prior to solder mask to make the fill even with the PCB surface.
- Abnormal Legend height - Lump
- Solder mask too thick & off set
Suspect BGA Device Sitting on whit marking (thick) ink and creates more gap. The last print height prior to under wiping the stencil is lower than the first print. Stencil thickness is 4 mil (0.1mm). If the paste print is less than 4 mil there is possibility of not enough paste contact with micro BGA further aided by white marking legend height.
If the **total height** from PCB laminate to legend is competing the BGA Ball, there is possibility of co-planarity issue. Paste & Ball can melt separately. Some cases partial paste would melt with ball and some on the PCB pad due to co-planarity effect.

<table>
<thead>
<tr>
<th>Coating Thickness as seen in the Bare PCB (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Surface</td>
</tr>
<tr>
<td>PCB Pad</td>
</tr>
<tr>
<td>Solder Mask as in this PCB</td>
</tr>
<tr>
<td>Via Hole Fill</td>
</tr>
<tr>
<td>Legend</td>
</tr>
<tr>
<td><strong>Total height Created</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Probable Height After Paste Print (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Surface</td>
</tr>
<tr>
<td>PCB Pad</td>
</tr>
<tr>
<td>Solder Paste (5 mil stencil)</td>
</tr>
<tr>
<td>Sphere Height upon placement</td>
</tr>
<tr>
<td><strong>Total height Created</strong></td>
</tr>
</tbody>
</table>

If the total height from PCB laminate to legend is competing the BGA Ball, there is possibility of co-planarity issue. Paste & Ball can melt separately. Some cases partial paste would melt with ball and some on the PCB pad due to co-planarity effect.
Diagnosis

- Suspicion on print volume (insufficient) eliminated
- Print quality appears to be good
- PCB solder mask misalignment – Noticed
- Via hole fill is not co-planar.
- White marking legend – too thick
- Combination of mask & legend create gap between the board and stencil
- That is why paste bridging noticed adjacent mBGA
Recommendations: PCB

- Via-hole fill could be by resin instead of solder mask
- Via-hole fill has to be flat
- The advantage of resin is that it can be leveled after curing by buffing or brushing.
- *Legend ink marking can be thin or removed*
- Removal of white legend recommended across the board especially over BGA
- Solder mask registration should be uniform around the pads. 0.1 mm uniform all around the BGA pads desired. A lot of shift seen.
- *Assembler also does not need white marking on this side*
Results:

- Boards with the above modification in Solder mak & Legend now being assembled for last 10 months (Average 1 million PCBs / Quarter)

- No complaints - Zero Defect on mBGA locations

What did we learn?

The Thickness of a Piece of Paper Can Be the Difference Between 100% Rework or High Yields
Wetting Issue at an EMS ...........
PAD contamination /White residue on PAD (due to higher surface tension it created solder ball on PAD after reflow process)
Rework @ Legend Printing

White mask residue and solder lump

Not solder due to white residue on pad
Rework – at Legend Printing & its Effect
Issues 2: Contaminated PAD

Suspected green mask ink/residue on PAD

PAD Contamination and white residue on pad

Suspected ink/residue on PAD
Solder mask
An Experience with a large handset manufacturer......

1. PWB ‘C’ solder mask resist clearance is good compared to other 2 makes PWB.
2. After optimizing the print parameters we found good result in C compared to A & B.
3. In XXXXXX product we are using only ‘C’ make PWB’s from the start of the product, our PPM level for this component (0.4mm CSP) is low 300-350PPM.
Difference between the PWB’s

XXX XXX (0.4 mm CSP) Solder Short Trend for Different PWB’s

<table>
<thead>
<tr>
<th></th>
<th>Series 1</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4767</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>1011</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>354</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Quality of via’s varies by supplier

Handset MFR: PWB Supplier 2 - Cxxxxxxx
Handset MFR: PWB Supplier 3 - Axxxxxx
Test Run 10/17 – 4 Lots from One Supplier

Lot Number 3806

Lot Number 3706

Lot Number 390A

Lot Number 400A

Pads= 220u Apertures= 245u (square)
Take Aways

• Quality of via’s varies by supplier

• **When via’s were too large and not centered the defects increased**

• Quality of PWB’s varies within supplier samples

• PCB-2 was shipping mixed lots within packs of 50 PWB’s

• 0.4 mm component placed after paste inspection – this was a change made for .4mm production
Solder Mask Mis-registration

When implementing fine-pitch BGA/CSP components into production, some process issues can be caused by solder-mask mis-registration that occurred at PCB fabrication.
A completed PCB assembly with solder shorts under fine-pitch BGA/CSP components caused by solder mask mis-registration can be difficult to detect with standard X-ray processes.
Soldermask Openings / Bridges

There is an obvious risk when placing a via hole too close to a SMD pad. If the soldermask and via hole moves towards each other during the manufacturing process there is a risk that the via hole is exposed. The solder will creep down the hole in the soldering process and give a bad soldering result.
The distance between the soldermask opening and hole edge should be at least 0.20mm to ensure that the hole is covered with soldermask.

With this design the solder will not creep down the hole in the soldering process and give a bad soldering result.
Soldermask Openings / Bridges

Note: Cu thickness ≤ 35µm and not including Immersion Sn finish.

**GENERAL**
- A = 160µm
- B = 230µm
- C = 65µm
- D = 100µm

**MODERATE**
- A = 125µm
- B = 200µm
- C = 50µm
- D = 100µm

**ADVANCED**
- A = 100µm
- B = 150µm
- C = 37µm
- D = 80µm
Board Layout - Yield Driver

- Maintain .010 min. pad
- Min. mask stripe .004
- .003 mask clearance

If SMT pad to pad spacing is less than .010 – mask stripe less than .004 may cause manufacturing issues, “window” mask clearance may be required.

Solder Mask Feature Size
Soldermask Openings / Bridges

Remove soldermask bridges when the pitch is too small
Soldermask close to the Pads

CAN CAUSE GASKETE

Recommendation

For Ni-Au; Immersion Sn & Ag; OSP

-50µ
Solder Mask Positional Accuracy is Not OK. There is a mis-registration of solder mask. Though there is no solder mask on Pad, still, this is a Recipe for MCSB.

Hot Air Solder Level (HASL) surface finish is not flat or non-co-planar. This can add further woes to the poor solder mask design.
More Solder Mask Mis-registration Issues

Solder Mask Positional Accuracy is Not OK. There is a mis-registration of solder mask. Though there is no solder mask on Pad, still, this is Recipe for MCSB

Hot Air Solder Level (HASL) surface finish is not flat or non-co planar. This can add further woes to the poor solder mask design
Mechanism of MCSB Formation due to Poor Solder mask Registration

Printing status:

Miss alignment on printing

After reflow:

No dissociation during the liquidus… return to the pad
With Solder mask closer to Pads

Printing’s:

Solderpaste on soldermask

Solderpaste Dissociation’s

Mid Chip’s
Good Soldermask Design Can Solve It

Big Gap > 120µ Required

No Reduction: 1/1
Good Soldermask Design Solves It

No solder Resist in Between

Solderpaste

0.61 mm

0.537 mm

Aperture: 0.51 x 0.35 mm

0.3 mm

25 µ

0.050 mm

No Reduction: 1/1

Good Soldermask Design Solves It
Another Field Example
Vendor: **XXX Germany**
Soldermask around R2 pads well-centered - **Acceptable**

Vendor: **YYY Local**
Soldermask though not on pads it is close to pads un-evenly around the pads. *(Soldermask mis-registration)*

*“No mask on pad”, “Acceptable as per IPC STD” Cannot help to solve the issue.*
Pad or stencil design can reduce MCSB rate

Examples of promising designs for reducing solder beading rate

- Pad spacing wider than pad spacing
- Trapezoid aperture
- Aperture with reduced center width
- Pad narrower than chip width
- Thinner stencil
- Bow tie pattern
- Home plate pattern
- Recessed inner edge
<table>
<thead>
<tr>
<th>Defect</th>
<th>Photo</th>
<th>Stencil Design</th>
<th>After DfM Design</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid Chip Solder Balling</td>
<td><img src="image1" alt="Image of Mid Chip Solder Balling" /></td>
<td><img src="image2" alt="Image of Stencil Design" /></td>
<td><img src="image3" alt="Image of After DfM Design" /></td>
<td>- R/C Chip</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Medial 25% Cut</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Solder Ball prevention</td>
</tr>
<tr>
<td>Solder Bridging at QFN Pads</td>
<td><img src="image4" alt="Image of Solder Bridging at QFN Pads" /></td>
<td><img src="image5" alt="Image of Stencil Design" /></td>
<td><img src="image6" alt="Image of After DfM Design" /></td>
<td>-- Medial PAD Cut : Hourglass shape application</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Inside 0.18 mm, outside 0.195 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Dummy PAD : Medial 10% Cut Hourglass shape DNA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Reverence (the way) 5% extension</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- A Round (Oblong) outside application</td>
</tr>
<tr>
<td>Slitting of Heat Sink area</td>
<td><img src="image7" alt="Image of Slitting of Heat Sink area" /></td>
<td><img src="image8" alt="Image of Stencil Design" /></td>
<td><img src="image9" alt="Image of After DfM Design" /></td>
<td>A : CAD PAD width</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>B : 1/4 Cutting work</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C : Mask reinforcing band width (1.0 mm)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D : Outside :</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.3 mm</td>
</tr>
</tbody>
</table>

(DfM Study) Solving Process Issues Examples
BGA Less Solder Issue – another field example

Good Solder mask spacing around pads

Poor Solder mask spacing around pads – a recipe to create soldering disasters.

(mis-registration of PCB Vs Mask layer film during solder mask exposure process)
Bridging

Good Design For Manufacturability as IC pads are shaved in between and additional space created to prevent bridging (PCB-C)

Bridging observed more in PCB-B PCB. Space when measured found to be less by 30-50 microns when compared to PCB-C. Solder Mask in between pads can be removed.
Solder Mask Opening Design

Pad Geometries

- Non-Solder Mask Defined (NSMD)
  - Size of Pad Defined By Copper Pad and Interconnections (Variable Size)
  - Solder Encapsulates Pad
  - Limited to Components With Lead Pitch Greater Than 0.4mm

- Solder Mask Defined (SMD)
  - Size of Pad Defined By Solder Mask Opening (Uniform Size)
  - Solder Covers Exposed Pad (Fills Opening)
  - Required For Components With Lead Pitch 0.4mm or Less.
  - Preferred for Leadless Array Devices Like LGA’s, Multi-row QFN’s, etc.
On both PCB’s and the package’s substrate, there are two primary pad configurations for BGA solder ball attach: Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD). SMD pads allow the solder mask to touch the pad. NSMD pads limit the solder mask to outside of the pad area, (Figure 1). With SMD pads, a smaller ball to pad interface is achieved resulting in a less robust connection. Also, it has been shown that the sharp edges of the solder mask in SMD pads can initiate solder joint cracking at the ball to pad interface. When available, devices with NSMD substrate pads should be chosen. PCB layout should always use NSMD pad design for BGAs. The manufacturer’s recommended pad size should be used.
Solder Mask Selection

Matte Finish Solder Mask Has Increase Surface Energy To Hold Flux To The Board (More Flux For Solder Joint Formation)

Dull/Low Reflection Appearance

Glossy Finish Solder Mask Has Low Surface Energy to Flux To The Board (Less Flux For Solder Joint Formation – Solder Balls, Icicles, Flags, etc.)

Highly Reflective Appearance

Preferred

Not Preferred
Hot Air Levelling Issues at Assemblies
Objective

- To establish the root-cause analysis for poor FPY at ICT for 722k LF STB PCBs for a major EMS in India
- FP Yield dropped to ~60% vs 85% recorded till then

<table>
<thead>
<tr>
<th></th>
<th>Aug'10</th>
<th>Sep'10</th>
<th>Oct'10</th>
<th>Nov'10</th>
<th>WW48</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stages</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSI</td>
<td>99.30%</td>
<td>98.87%</td>
<td>99.39%</td>
<td>99.54%</td>
<td>99.68%</td>
</tr>
<tr>
<td>TSI</td>
<td>99.25%</td>
<td>98.96%</td>
<td>99.07%</td>
<td>99.25%</td>
<td>99.46%</td>
</tr>
<tr>
<td>SMT ICT</td>
<td>98.00%</td>
<td>97.11%</td>
<td>97.39%</td>
<td>97.86%</td>
<td>97.46%</td>
</tr>
<tr>
<td>Wave VI</td>
<td>98.50%</td>
<td>97.66%</td>
<td>98.05%</td>
<td>98.26%</td>
<td>97.93%</td>
</tr>
<tr>
<td>TH Hole ICT</td>
<td>95.50%</td>
<td>96.22%</td>
<td>97.19%</td>
<td>95.94%</td>
<td>91.82%</td>
</tr>
<tr>
<td>Combi</td>
<td>95.50%</td>
<td>95.54%</td>
<td>95.98%</td>
<td>96.18%</td>
<td>96.16%</td>
</tr>
<tr>
<td>Final VI</td>
<td>99.00%</td>
<td>98.84%</td>
<td>99.12%</td>
<td>99.30%</td>
<td>99.42%</td>
</tr>
<tr>
<td>Overall FPY</td>
<td>86%</td>
<td>84.31%</td>
<td>86.94%</td>
<td>87.04%</td>
<td>82.96%</td>
</tr>
</tbody>
</table>

Production:

- Aug'10: 42,330
- Sep'10: 86,502
- Oct'10: 41,296
- Nov'10: 38,049
- WW48: 15,180

FPY Trend:

- Aug'10: 84.31%
- Sep'10: 86.94%
- Oct'10: 87.04%
- Nov'10: 82.96%
- WW48: 61.15%

Overall FPY:

- Aug'10: 86%
- Sep'10: 84.31%
- Oct'10: 86.94%
- Nov'10: 87.04%
- WW48: 61.15%
Background

- Extensive analysis has already been carried out & data captured by that EMS’ ME team for this poor FPY issue at ICT
- Upon completion of 3 thermal cycles (2 refloows + Wave), ‘Copper Exposure’ on test pads has been identified as the reason for poor contact for pins in the ICT jig.
- Test pads cleaned with solvent Bio Act SC-10 & Re-test did help to improve yields but only marginally.
- This issue was not observed until Date Code 4010 and 4210 when EMS started using those boards from Oct 10)
- There was no change in Date Code for SLS 65 Flux which was in use when DC 4010 & 4210 arrived.

Test pad appearance after the third thermal cycle (wave soldering). Test pins are unable to establish firm contact over exposed copper / oxidized pads.
Visual Inspection for bare PCBs

Problematic Date Code: 4410

HAL solder coating Thickness – uneven & virtually nil to 200 micro inches
Visual Inspection for bare PCBs

Found OK Date Code: 2610

HAL solder coating Thickness – Closer to 600 micro inches (15 microns)
The Distinct Difference between 2610 Vs 4410

- 2610: Flat, Co-planar, Thicker HAL solder Surface
- 4410: Uneven, non Co-planar, Thinner HAL solder Surface
Bare PCBs - thru Reflow 2 Times with Capton tape

Thinner 200 micro inches HASL Surface start eroding and paving base metal exposure

2610

Vs

4410

Pictures taken at similar locations on each date code pcb

Without tape
Same PCBs – thru WAVE without Flux

Comparison

Thinner 200 micro inches HASL Surface start eroding and paving base metal exposure

2610

Vs

4410

Pictures taken at similar locations on each date code pcb

Thicker 600 micro inches HAL solder Surface stable at it’s location not exposing copper

With tape

Without tape

Vs

With tape
With SLS 65 Flux thru Wave Fluxer ON

2610 Date Code with Tape on

4410 Date Code with Tape on

It proves beyond doubt that flux has no role play for HASL coating getting receded during thermal excursions

Pads Exposed to Flux
HASL – a major variability

Major cause of the BGA solder joint failure is observed due to poor HASL finish of PCB.

1. Co planarity – Uneven solder surface
2. Too thin coating of HASL leading to migration after 1st reflow itself exposing copper. (Poor solder ability in the subsequent reflows)
3. Solder mask window uneven around the BGA pad.
What do experts say about HASL thickness?

Bob Willis is a process engineer providing engineering support in conventional and surface mount assembly processes. He runs special production features at exhibitions and offers his seminars, workshops and PCB manufacture and assembly audits worldwide. www.ASKbobwillis.com

The results in Figure 8 are XRF measurements taken from sample boards during a SMART Group hands on workshop conducted in 2006. The boards featured a range of different pitches.

As a guide the following specification may be useful. It can used or modified for solder levelled boards. Further inputs to improve these suggestions are always welcomed by the author.

If specified all exposed outer copper surfaces shall be coated with solderable finish of tin/lead or lead-free on the surface of mounting pads, test points and plated through hole. The coating should provide a minimum of 12 months shelf life and meet the solderability requirements of the IPC or IEC standards using a wetting balance. The coating thickness should average at between 10-15 µm on specified pads.
What do experts say about thickness?

The quality and consistency of the solder leveling process could be far better than some of the examples in the industry. Often the variation on coatings is down to the time spent on setting up the process for different designs. The PCB industry could have done better even with vertical leveling systems as has been demonstrated by sub-contracting leveling services like CEMCO. The leveling process over the last 10 years has been demonstrating satisfactory coatings for lead-free in recent trials on tin/copper/nickel boards for the SMART Group workshops and production lines.

As a guide the following specification may be used or modified for solder coated printed boards:

If specified, all exposed outer copper surfaces shall be coated with solderable finish of tin/lead or lead-free on the surface of mounting pads, test points and plated through hole. The coating should provide a minimum of 12 months shelf life and meet the solderability requirements of the IPC or IEC standards using a wetting balance. The coating thickness should average be between 10 – 15um on specified pads. The coverage in the plated through hole should be with a minimum of 3um on the knee of the plated through hole. The solder leveling process should not affect the minimum hole size requirements.

The thickness of the coating should be tested using XRF measurement for thickness and coating composition. Regular solder samples should be taken to control the build up of copper in the solder bath which will affect the solder reflow temperature. Panels should not be leveled twice due to the possible impact on copper dissolution on through hole plating.
### Wetting characteristics of the Cu, Cu₃Sn and Cu₆Sn₅ surfaces

<table>
<thead>
<tr>
<th>Material /Flux</th>
<th>Wetting Angle (°)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu/RMA</td>
<td>3</td>
<td>72</td>
</tr>
<tr>
<td>Cu/R</td>
<td>16</td>
<td>19</td>
</tr>
<tr>
<td>Cu₃Sn/RMA</td>
<td>10-15</td>
<td>26</td>
</tr>
<tr>
<td>Cu₆Sn₅/R</td>
<td>93-101</td>
<td>4</td>
</tr>
<tr>
<td>Cu₆Sn₅/R</td>
<td>10-17</td>
<td>23</td>
</tr>
<tr>
<td>Cu₆Sn₅/R</td>
<td>180</td>
<td>0</td>
</tr>
</tbody>
</table>

*Note that:*

- **RMA**  Activated rosin flux
- **R**  Non-activated rosin flux

**Side view shadowgraph of the areas spread tests on Cu, Cu₃Sn and Cu₆Sn₅ using two different fluxes**

**Side view shadowgraph of the areas spread tests on Cu₆Sn₅ after pre-oxidation at 235°C for various times**

**Conclusions:**

1. The wetting of the Cu₃Sn and Cu₆Sn₅ is poorer than Cu.

2. **A strong degradation of the wetting of the intermetallic occurred with increased oxidation**
   
   *(SnO₂ and SnO was identified as a primary oxides formed on Cu₃Sn and Cu₆Sn₅ during storage in air)*
The metallurgy

Optical images of the cross sectioned board with HASL

The areas with thin coating would have insufficient wettability after aging due to exposed intermetallic (IMC growth rate much slower at room temperature compare to the elevated temperatures, but still reaction does not stop.

If solder layer was too thin, all tin would be consumed by Sn/Cu interfacial reaction)
We verified at our lab using Micro-section equipment & SEM equipment and found that HASL thickness is less than 5 microns (200 micro inches) and IMC thickness is around 1.3 micron.
Observations

- The HASL surface finish is non-uniform, with exposure of copper and very thin layers of HASL in some areas.

- Residual oxides on the surface of the HASL may prevent proper wetting, or form weak inter-metallic interfaces when reflowed.

- Oxidation of Test points – an hindrance at ICT. Poor FPY is attributed to this issue.

- Application of a more uniform HASL surface will assure complete coverage of the underlying pad and will alleviate the exposure of the underlying copper, while reducing the risk of oxidation.

- Can overcome this issue with the HASL original thickness Spec of 400-600 micro inches (10-12 microns) as observed in Date code 2610

- PCB Supplier accepted this as an issue and their subsequent supplier with nominal HASL thickness made the ICT yields back to normal.
Wave Solder & Rework Issues

Limit Effects Of Copper Dissolution

- Use Lower Dissolution Rate Solder Alloy
  Modified SAC Alloy (Sb, Ni, Zn, Ge, In, Etc)
  Non-SAC Alloy (Sn/Cu/Ni, Etc)

- Pad Trace Connection
  - Tear Drop
  - Snow Man Connection
  - Wide Trace
  - Greater Than 0.010”

0.005” Trace Dissolution in 30 Seconds

- PCB Photo Courtesy of Cookson - Alpha Metals
  Cryns, Jean & Lee, “Copper Dissolution Rate in Pb-Free Soldering Fountain Systems”, SMTA-I 2006

Original

SnPb

SAC 305

SN100C

After wave soldering, 265°C solder temperature, 12 seconds contact time

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More Encounters at other EMS

These surface imperfections (non-coplanar surfaces) will lead to creation of gap between stencil and PCB (increase off-contact distance) and also between components and pads to be soldered resulting bridging at adjacent fine pitch components, poor solderability causing re-work.
Solder lump and BGA PAD contamination
HAL Surface Finish Co-Planarity

Thin coatings HAL thickness less than 5 microns will lead dissolution of coating into copper. As micro level copper exposure is prone oxidation faster aided with multiple temperatures in the processes, the surfaces will become difficult to solder. Spreading will be poor. Non-wetting or de-wetting will be the result.
HAL Surface Finish Co-Planarity Issues
On Hot Air Levelled Boards

Solderpaste Sliding

- Solderpaste
- HAL plating cambered
- Soldermask close the pad
- Solderpaste on the soldermask… mid chip balling!
Top Contributor for Resistor Pack Defects

PCB Surface Finish CO-PLANARITY (HAL)

16. SURFACE FINISH: HOT AIR SOLDER LEVEL (HASL), 100% COVERAGE PER ASTM B-579. FINISHED SURFACE TO MAINTAIN COPLANARITY WITHIN 0.002.
Combination of Poor pad design, non-coplanar HAL & Placement off-set.

**Component Leads not touching the paste “Floating”**

(Overcame with Stencil modification temporarily)

Resistor Pack should have been placed above
Combined Effect of PCB Surface Finish (HAL) & Placement

Component Leads not touching the paste "Floating"
Resulting "Not Soldered / Less paste after Reflow"
Disadvantages of HASL?

Variation in Coating Profile

This problem can be minimised by adjustment of process parameters.
More HAL PCB related Issues

Solder Ball in Via and solder Chips Nearing QFP

Excess Solder or Ball on Fiducial
Solder Ball in Via and solder Chips Nearing QFP

Solder lump near the QFP creates a gap between the board and stencil (snap-off or off-contact distance increased).

The Effect upon Printing
More HAL PCB related Issues

Design aspects

HASL (Leaded and Lead-Free)

There is not so much design concerns about this surface treatment.

C. Solder balls.
Holes plugged from only one side (partially plugged) with soldermask can entrap solder that the air-knives cannot remove from the surface (force it into the partially plugged hole). These solder balls may become dislodged and re-deposit onto the surface during the reflow operations.

D. Edge plating on thick boards
We have experienced issues on thicker boards with edge plating, where the edge plating has been found to become loose after the lead-free HASL process.
More HAL PCB related Issues

Quality aspects

HASL (Leaded and Lead-Free)
With lead-free solder, quality control is more critical than with traditional SnPb HASL.

A. Control the alloy.
It is critical to have good control over the alloy so all elements are within limits, the new Pb-F alloys dissolve more copper from the boards.

B. Use good flux.
Many of the low-cost fluxes struggle with the heat and may perform badly.

C. Maintenance on machinery
The Pb-F HASL’s are more challenging to wet on the surface and are also much more easily to ‘blow off’ during processing so that thin layers provide insufficient pure tin and limits storage time and solder cycles.
As the board comes out of the solder, air knives blast it on both sides, leveling the solder on the pads.

This, however, can cause problems during assembly:

Bad air knives leave an uneven pad surface so components cannot lay flat.

The solder in the hot air leveler is contaminated by a tiny amount of copper from each board. The solder left on the pads thus becomes less solderable.

Too much time in the solder pot creates a thick layer of intermetallic alloy, which weakens joints made in assembly.
Immersion Tin

There are some design concerns about this surface treatment.

**A. Contamination**
Since this treatment is very sensitive to contamination, holes plugged from one side (partially plugged) are not recommended. See right hand image.

Also holes very close to SMD pads are not recommended, since the plating solution will be trapped inside and can contaminate and destroy the solderability.
Tombstoning

• It’s been said only 0.2 seconds of time difference in wetting at the each terminal can cause tombstoning.
Manhattan Effect...?

Tomb stoning

Viagra.

Courtesy: Gilbert Renaud, Global Applications Manager
Tomb Stoning @ R12 at an Indian OEM

Poor Apertures and Pads Design

Different pad sizes for the same component
Bad Pad Design

30% in the Pads

A recipe for tomb stoning.................
Good Pad Design to avoid Tomb Stoning

70-50 % in the Pads
Contamination on surfaces

Crystal Component in a thumb drive at large OEM in Delhi
2a. Solder mask shift observed (impact of this could be MCSB) too close to pads

2b & 2c, 2d, 2e, 2f, 2g Contamination on pad surfaces could lead to poor solderability

Visual inspection for OSP is though in the edge of acceptable range it is still a process indicator. Contamination on rollers, improper cleaning of OSP holding tank, handling & re-work are few potential causes.
Observations

- In general the coating appears oxidized & thin
Un populated PCB - B

Solderability ?
OSP Visual Inspection

Preferred Coating Appearance
Uniform, matte pink color

Acceptable Coating Appearance
Slightly darker, striated, or spotted

Not Acceptable Coating Appearance
Extremely dark

Not Acceptable Coating Appearance
Crystalline or foreign material
Effect of Board Thickness on Topside Fillet formation

- Board thickness increase thermal mass of plated through-hole
- Increase thermal pad isolation to improve solder flow to the top side
- Increase lead hole clearance (aspect ratio) to improve solder flow to top side
What To Do?

• Increase Solder Temperature?

Lead Free Solder Issue
Higher Solder Temperatures Or Increased Solder Dwell Times Create Problems With Pads On Solder Side

* Dr. S. Zweiger, Solelectron GMBH, Productronica Green Day, November 2005
Effect of Thermal relief for Hole-Fill

Via/Pin With Thermal

Via/Pin Without Thermal

Figure 1-14 A connection to a plane layer through a thermal relief.
PCB Impact on Process Performance

- Copper Plane
  - Uniform Thickness
  - Balanced Thickness To PCB Centerline

- Thicker Copper Plane Layers Increase Thermal Mass
  - Thinner Is Better
  - Increase Thermal Pad Isolation

- Issues Include:
  - PCB Warping
  - PTH Hole Fill
Effect of Lead Length on Topside Fillet formation

- Lead Length protrusion too long on solder side:
  - Only a small quantity of solder retained in soldering area, solder flow downwards along component lead

- Lead Length protrusion too short on solder side:
  - Only a small quantity of solder can transferred, and the heat transfer maybe insufficient
Micro-Via in Pad

- Voids in Solder Joints
  - Unfilled Via in Pad

- Provide Flat Pad With Filled/Plated Closed Via

- Solder Joint Formation
  - Thermal Connection
    - Plane Connection
    - Multiple Connections
    - Stacked Via
  - Solder Volume
    - Via Location - Edge

No Via

Unfilled Via’s

Plated Closed & Filled Via
Factors in Voiding

Defect: Big Void in BGA Joints
Plating Issues?

Copper is very thin. Is there a copper open?

Plating gap? Any outgasing from the gap?
Factors in Voiding

Fig. 2 Illustrates the cross-sectional analysis of the locations marked in the X-ray images.
Factors in Voiding

Failure Mode:

- Cross section found plating disconnection and plating gaps at the pad.
- Vapor from through hole can get out to make a void during reflow process.
Factors in Voiding

Configuration of BGA & Pad:

Cross section found plating disconnection and plating gaps at the pad. They cause voids in BGA joints.

Resin in through hole. Vacant through hole and broken pad were found.
Addressing Issues that Affect Voiding in Lead-Free Solders will Deliver Increased Process Yields

- Voiding is found with ALL solders!
  - SAC305 gives lowest voiding of tested Lead-Free solders.
  - Not a reliability issue.....until 0.5mm pitch.
  - Improvement in solder paste flux chemistry is reducing voiding in Lead-Free Solder paste.

- Determine the voiding levels on a range of
  - Boards used.
  - Component types used.
  - Component finishes used. Determine if these are the same finishes that will be used after the transfer to Lead-Free.

- Voiding occurs at the interface between solder and pad.
Component Issues - Decreasing Pitch

Potential Issues:

- Paste Volume Control
- Component/PCB Flatness
  - Internal Split Plane
  - NFP Removal Impacts
- Component/PCB Warpage
LGA/QFN Package Assembly

- Trace Routing Under Component Create Localized Height Variations
  - Standoff Height Variation

- Leadless Devices Are More Sensitive To PCB/Component Flatness/Warpage
  - Received Condition
  - In-process Condition (During Reflow/Rework Solder Process)
Warpage & Thermal Profile Issues

May Require Change In Production Process
(Increased Solder Paste Volume Application, etc. Reflow Pallets For Board Support)

• Tooling To Bridge Warpage Gap.
(Decreased Thermal Change Rate And Delta T Vertically In Component Package – Reduce Surface To Cooler Location Temperature Delta - TCE Induced Warpage)

• Reflow Profile To Bridge PCB Warpage Gap.
(Decreased Thermal Change Rate And Delta T Vertically In PCB – Reduce Surface To Cooler Location Temperature Delta - TCE Induced Warpage)

Large ΔT across Board

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PCB Fabrication Variation

Pad Size Comparison
- Same design data may not yield same PCB pads sizes.

Hole Fill issue due to Solder mask Residues at an EMS

Richard Puthota
Alpha India
Aug 2012
RF Tuner

Ideal Hole-Fill

Partial Hole-Fill
The Solder Mask Residues....

The via holes tenting using solder mask seem to be improper. Either the exposure level in UV is less or curing of solder mask in the oven does not seem alright. Suspecting the developing process of solder mask too. That is why flakes are seen on the surface and some tenting holes are broken. There is every chance that the PTH barrel is contaminated with the mask residues which can be a potential challenge for hole-fill.
Oxidation

Effect:
- Possibility for pad lift due to weak joint on one side
- Poor solderability due to oxidation on pads
Commonly Observed Issues in the Field...(OEMs & EMS)

WE CAN EASILY OVERCOME – AT NO EXTRA COST FOR QUALITY

• Legend Printing / Via Hole Fill / Tenting - Think of CO-PLANARITY

• Rework @ Legend Printing - Need Clean surfaces – Review PROCESS

• Pad definition versus Solder mask definition – DFM with Gerber

• Solder mask Printing Accuracy – EASY....Registration at Exposing

• Surface Finish – CO-PLANARITY!

• Effect of Thermal relief for Hole-Fill – DFM

• Residues / Oxidation – Barriers for Soldering, Look into your processes.
Closing Thoughts

Good raw material of boards is one of the most important parts of high yield surface mount assembly

A person who never made a mistake never tried anything new.

No problem can be solved from the same level of consciousness that created it.

We cannot solve our problems with the same thinking we used when we created them.

Albert Einstein
Closing Thoughts

Engage with your Customer

Delight your Customer

Gandhi Quote: Customer Focus

“A customer is the most important visitor on our premises, he is not dependent on us. We are dependent on him. He is not an interruption in our work. He is the purpose of it. He is not an outsider in our business. He is part of it. We are not doing him a favor by serving him. He is doing us a favor by giving us an opportunity to do so.” - Gandhi