PCBA Design Guidelines and DFM Requirements

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“Guidelines” and “Requirements” are what those who design PCBAs have to learn to deal with…but when, where, what, why and just how much do we get involved?

- Waiting until there is wet solderpaste on the board is a little late to find problems.
- Having an unplanned re-spin of your PCB is never easy to explain.
- Missing a critical release date is even more difficult.
- Will this presentation give you all the answers?
- No. But you may learn enough to get you pointed in the right direction.

DFM = Risk Management

Aka: Insurance
WHAT YOU ALREADY KNOW –

- Your company has Internal Design Guidelines
- Your Service Bureau has their Design Guidelines
- IPC has Everything You Need...
- Combination of both worlds:
  - Use IPC docs customized with exceptions for your application

http://www.ipc.org/4.0_Knowledge/4.1_Standards/OEM-Standards/IPC-OEM-Stmtd-A4-English-1111-ONLINE.pdf
IPC-7351 Section 16. ZERO COMPONENT ORIENTATIONS

- Standardize components with respect to CAD library
  - Schematic
  - Physical part
- Normalizes the pin numbering
  - Pin 1 is the cathode
  - Pin 1 is the “+”
  - Pin 1 is first pin

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IPC-7351 Figure 16-1 lists the most commonly used parts and their proper zero component rotation (pps. 96-102)

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How do we get involved? ➔ Early Engagement Timeline

- DFM panel Review
  - DFT test fixture review
- DFT review for test hooks & part technology
- DFC unique components test & mfg strategy
- DFM w/Valor™ process review
  - DFT access review
  - Final BOM review
- DFM/T performing Valor™ Review on CAD & BOM data

Early Engagement Timeline:

1. First Look BOM
2. Schematic
3. Physical PCB Parameters
4. Preliminary Layout
5. Data Release
6. Prototype Build
7. Ship

Process Development
Tools for DFM

What should you use?

Experienced DFM engineer
Mentor Graphics Valor™
Polliwog Corporation
PCB Design Review Solution (PollEx-PCB)
Valor Parts Library (VPL)

VPL contains more than 35 million commercial electronic component part numbers

- Accurate graphical contour
- Pin contact areas and positions
- Dimensional tolerances
- Overall dimensions including height
- Pin 1 identification

Assembly Review - merging the database with complete BOM and AVL may identify manufacturing issues related to:

- Component to Component spacing
- Component to Board outline spacing
- Pin to Pad spacing using VPL
- Padstack Analysis (spacing to vias and other board features)
- Provide Assembly Process and Panel Strategy assumptions
- Recommend fiducial and tooling hole requirements
- Solder mask check
- Pads for Drills check
- Review general Assembly and Fabrication drawing notes
- Identify manufacturing tooling required like: stencils, AXI pallet, rework nozzles, and selective wave pallets, etc
- Component quantity matching (BOM Manager)
- Report parts on BOM that are not in the layout
- Report parts on board that are not in BOM (non pops)
“You don't know what you don't know”
Types of Defects

- **Manufacturing Defects**
  - Missing component
  - Misplaced component
  - Insufficient solder
  - Solder bridge/short
  - Open solder joint
  - Electrically def comp
  - Reversed Component
  - Bent Pins

- **Design Related Defects**
  - Affect processes
  - Impact yield

![Case Study -- Average Defects per Board
14 month production period](image-url)
- **Design Related Defects**
  - J10 is 4” long
    - SMT feeder
    - Hand placed

**Hand placement of SMT components ➔ Increased defects**

**J11**: 160-pin Samtec SMT connector is machine placed

**J10**: 240-pin Samtec SMT connector must be hand placed
Design Related Defects

- BNC connectors J17-J22 have discrete chip components too close to pins.

- Reduced opening for BNC lead exposure to wave.

- Notice thin wall next to 0402.

- Titanium insert covering 0402 SMT chip next to pin.

- 10 mil pad-to-pad space.

- Missing components.

- Bottom View of PCB after 1st Side SMT.

- Pockets to clear SMT components.

- Reduced opening around TH pins.

- Maximize opening around TH pins.

- Selective Solder Pallet Top View.

- Selective Solder Pallet Bottom View.
DFM Case Study ~ AFTER

Case Study ~ BEFORE Selective Wave Pallet

Case Study ~ AFTER Selective Wave Pallet

Larger Opening

Exposed Center Pins

Less Complex Insert

More Space
- Encroached soldermask, plug, or plug and plate to prevent solder movement between sides of the PCB during reflow
- Critical when these packages are mirrored on opposite sides
QFN Center Thermal Pad

- Maintain spacing between thermal pad and perimeter pads (~15 mils)
- When thermal vias chose one of these options
  - Plug and plated vias (preferred)
  - Place vias outside perimeter of the thermal pad
  - Cover or plug vias with soldermask

Example QFN24 4mm x 5mm w/ .5mm pitch
(As viewed through top of part)

Alternate Thermal Pad Design with 9 Vias
- Rule for clearance size is \textit{feature size + 6 mils}
- Open both sides
- Prevents volatile entrapment
- Encroachment ensures adequate soldermask web
- Rule for clearance size is \textit{finished drill size + 6 mils}
Preferred Board Shape

- Automated equipment requires 2 parallel sides

When this condition is not met breakaway features must be added.
Be careful the word “Panel” is audience sensitive

- **Assembly**: A single PCB with breakaway features or a multiple-up array
- **Fabrication**: A process panel comprised of multiple finished PCBs

- Customer control drawing should show the finished PCB only
- “Panel” is assembly process related ➔ “Assembly Array”
- Optimized for fabrication material usage and assembly handling
PCB Panelization (aka: Assembly Array) Basics

- Design requires evaluation of
  - End product requirements
  - Assembly process
    - Handling
    - Component placement and related processes
  - Depanelization ➔ “when” and “how”
- Fabrication process
- Affect on cost at each of these steps
Case Study ~ BEFORE

- Profile and SMT require breakaways
- 18” x 24” FAB panel
- 2-up at FAB house
- Panel usage 43%
- Cost per board = $634.86

KwickFit PCB Panelization Optimizer (www.micromeg.com)
Case Study ~ AFTER

- Remove breakaways
- Use SMT pallet
- 18” x 24” FAB panel
- 4-up at FAB house
- Panel usage 70%
- Cost per board
  =$341.60
- $293.26 (46.2%)
  PCB cost savings
- SMT pallets $179 each
  16 for 1st side
  16 for 2nd
- Total $5728.00
  (ROI after 20 boards)
11th Commandment of SMT PCB Design
“Thou shall not forget fiducials”

- Fiducials
  - Global
  - Local
  - Panel
Plated Through Holes (PTH) for leaded components

- Lead size to hole size
- Pad size
- Aspect ratio
- Soldering

Figure 7-108

Figure 7-109

Figure 7-111
Supported Holes

NFP ➔ PTH ➔ Multi-Layer PCB ➔ CTE

- NFP removal is industry standard practice
- Wave soldering TH pins
- CTE caused separation on layer 2 and lifted pads
- Restoring NFP on TH pins eliminated opens
Summary and Review

Analogy for PCB Design Process

© http://www.repair-home.com/how_to/home_construction_foundations.htm#Preliminary_Work
Thank You!

Glenn Miner is Benchmark Electronics Engineering Manager at corporate headquarters in Angleton, TX. He is now transitioning “30 something” years of experience in almost anything electronic, including circuit design, PCB design, fabrication, test, box build, low-to-high volume assembly, even oil & gas. Glenn is a DFM specialist with IPC C.I.D. certification and former president of the North Texas Chapter of the IPC Designers Council.