Package Thermal Performance

“What is Theta-JA?”

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Questions that are addressed:
• How hot will it get?
• How is the temperature rise predicted?
• How is the temperature measured?

Power dissipated in the die is conducted to the top surface of the package and to the board and then dissipated to the environment. Orange arrows show the heat flow.

\[ T_j \] “junction” or die temperature
\[ T_A \] Ambient or air temperature near the device
\[ T_B \] Board temperature at the edge of the device
\[ T_C \] Case temperature
One Dimensional Thermal Conductivity

\[ Q = \frac{k \cdot A \cdot (T_1 - T_2)}{L} \]

or

\[ \frac{(T_1 - T_2)}{Q} = \frac{L}{k \cdot A} \]

- **Q** - Heat dissipated (watts)
- **k** - Thermal conductivity  W/m K
- **T** - Temperature
- **A** - Area
- **L** - Thermal path length

A (area of conductor)

Thermal Resistance °C/W
Cooling: Convection and Radiation (and Conduction)

Convection: 

\[ Q = h \cdot A \cdot (T_S - T_F) \]

\[ h \propto (T_S - T_F)^{0.25} \]

Natural Convection \( h = 5 \) to \( 10 \) W/m\(^2\)K

Radiation:

\[ Q = \sigma \cdot \varepsilon \cdot A \cdot (T_S^4 - T_W^4) \]

Radiation heat transfer is about the same magnitude as natural convection

These equations are given in all the standard textbooks. \( Q \) is heat flow in watts, \( h \) is the convection coefficient, \( A \) is the area being cooled, \( T_S \) is the temperature of the surface being cooled, \( T_F \) is the fluid temperature, \( \sigma \) is Stefan-Boltzmann constant, \( \varepsilon \) is the emissivity of the surface, \( T_W \) is the wall temperature that is cooler than the surface being cooled.
## Electrical vs. Thermal Resistance

<table>
<thead>
<tr>
<th></th>
<th>Electrical Resistivity</th>
<th>Thermal Conductivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>$\rho = 10^{-6}$ ohm-cm</td>
<td>Copper</td>
</tr>
<tr>
<td>Typical plastic</td>
<td>$\rho = 10^{13}$ to $10^{15}$ ohm-cm</td>
<td>Typical Plastic</td>
</tr>
<tr>
<td></td>
<td><strong>20 orders of magnitude difference</strong></td>
<td><strong>3 orders of magnitude difference</strong></td>
</tr>
</tbody>
</table>

You can’t ignore the thermal insulators.
Thermal Resistance Measurement

• Assemble package with thermal die (special die with heater resistors and a temperature sensor (diode or resistor)

• Solder the package to the thermal test boards

• Apply power, measure the temperatures per the JEDEC specifications
Junction to Ambient Thermal Resistance (Theta-JA)

Standardized estimate of thermal performance on thermal test board

\[ R_{\theta JA} \text{ or } \theta_{JA} = \frac{(T_J - T_A)}{P} \]

Specifications

Test Method:
- JESD 51-2A

Test Boards:
- JESD 51-3
- JESD 51-5
- JESD51-9
- JESD51-10

One cubic foot enclosure, natural convection
Most Customers don’t use single layer boards, so …

Junction to Ambient Thermal Resistance (Theta-JA) on Multilayer Board (Usually 2 signal, 2 planes or 2s2p)

Example
196 15x15 MAP PBGA for 6.4 mm die size, 84ASA10536D001
Theta-JA (R_{0JA}) (1s board) 51 °C/W
Theta-JA (R_{0JA}) (2s2p board) 26

Both are JEDEC specified values (JESD51-2A and JESD51-6). You can find cases where each is the “right” answer. Make sure that you ask for and report both values.
Multiple Components on a Board

Natural Convection Results

<table>
<thead>
<tr>
<th>Thermal Resistance (°C/W)</th>
<th>Board Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>2s2p Board</td>
</tr>
<tr>
<td>52</td>
<td>1s Board</td>
</tr>
<tr>
<td>59</td>
<td>8 Pkg, 2s2p Board</td>
</tr>
<tr>
<td>104</td>
<td>16 Pkg, 2s2p Board</td>
</tr>
</tbody>
</table>

Theta-JA using JEDEC specifications are predictors of thermal performance.

Modeling of application is required.

Forced Convection 1m/sec from the right
Eight 119 14x22 mm PBGA on each side of board, 1 W each
Determine Junction Temperature for Customer

• Customers need to verify junction temperature for components in their application. The Thermal Characterization Parameter ($\Psi_{JT}$ or Psi-JT) meets that need. It varies slightly with air flow. We normally report natural convection values.

$$\Psi_{JT} = \left( \frac{T_J - T_C}{P} \right)$$

Thermocouple should be made with 40 gauge wire with both wire and bead attached to the top center of the package with thermally conductive epoxy. Test method defined in JESD51-2. Wire routed next to package body.
Junction to Case Thermal Resistance

\[ \theta_{JC} \quad \text{or} \quad R_{\theta JC} = \frac{(T_J - T_C)}{P} \]

Theta-JC is used to predict device performance with a heat sink

Specifications:
MIL-SPEC 883, Method 1012

Case thermocouple placed inside cold plate when tested at Freescale Thermal Labs

Cold Plate

Thermocouple

Thermal Grease between Package and Cold Plate

Other surfaces insulated
Junction to Board Thermal Resistance

For surface mount devices, most of the heat is dissipated to the board and then to the rest of the environment. Hence, the thermal resistance to the board is the most important thermal path. It is determined per the JEDEC specification JESD51-8.

\[ R_{\theta JB} \text{ or } \theta_{JB} = \frac{(T_J - T_B)}{P} \]

Board temperature measured with thermocouple soldered to trace at center of package

Requires 2s2p Test Board

Insulation
### Thermal Resistances (Quick Summary)

<table>
<thead>
<tr>
<th>Junction to Ambient</th>
<th>$R_{0JA}$</th>
<th>Single Layer Board</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient</td>
<td>$R_{0JA}$</td>
<td>Four layer board (2s2p)</td>
<td>commonly Used</td>
</tr>
<tr>
<td>Junction to Board</td>
<td>$R_{0JB}$</td>
<td></td>
<td>sealed box, or customer use in modeling</td>
</tr>
<tr>
<td>Junction to Case</td>
<td>$R_{0JC}$</td>
<td></td>
<td>heat sinks</td>
</tr>
<tr>
<td>Junction to Package Top</td>
<td>$\Psi_{JT}$</td>
<td>Natural Convection</td>
<td>determine junction temperature from thermocouple reading</td>
</tr>
</tbody>
</table>

\[ R_{0JX} = (T_J - T_X)/P \]
Application Environments ->

Which Thermal Resistance to Use
Junction Calculation Summary:

\[ T_J = T_A + P \cdot (R_{\theta JA}) \]  
Depends on board and local power density

\[ T_J = T_B + P \cdot R_{\theta JB} \]  
Sealed enclosures, board temperature dominates

\[ T_J = T_A + P \cdot (R_{\theta JC} + R_{\text{interface}} + R_{\theta SA}) \]  
With heat sink, include thermal resistance of interface material and sink to ambient thermal resistances

Validation of design using case temperature or determination of junction temperature at test or burn-in.

\[ T_J = T_C + \psi_{JT} \cdot P \]

These equations are simplifications. Heat flows more than one path which is not included in these equations.
Package Performance and Design
## Typical Leadframe Package Performance

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Enhancement</th>
<th>Name</th>
<th>Typical i/o Count</th>
<th>Description</th>
<th>Wire Bond?</th>
<th>Theta-JA (1s board) °C/W</th>
<th>Theta-JA (2s2p board) °C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOIC, TSSOP, SOP</td>
<td></td>
<td>Small Outline Package</td>
<td>8 to 32</td>
<td>Gull wing lead, two rows</td>
<td>Yes</td>
<td>65 to 150</td>
<td>45 to 90</td>
</tr>
<tr>
<td></td>
<td>HSOP, EP-SOIC</td>
<td>Heat Sink Small Outline Package, Exposed Pad</td>
<td>16 to 32</td>
<td>Die pad should be soldered to board</td>
<td>Yes</td>
<td>40 to 70</td>
<td>20 to 30</td>
</tr>
<tr>
<td></td>
<td>QFN</td>
<td>Exposed Pad Quad Flat No Lead</td>
<td>16 to 64</td>
<td>I/O pads are solder to board, Die pad should be soldered to Board</td>
<td>Yes</td>
<td>60 to 280</td>
<td>20 to 150</td>
</tr>
<tr>
<td></td>
<td>QFP, LQFP, TQFP, FQFP, PQFP, etc</td>
<td>Quad Flat Package</td>
<td>32 to 208</td>
<td>Gull Wing Leads, four sided</td>
<td>Yes</td>
<td>30 to 90</td>
<td>20 to 80</td>
</tr>
<tr>
<td></td>
<td>EP-QFP</td>
<td>Exposed Pad</td>
<td>32 to 100</td>
<td>Die Pad should be soldered to board</td>
<td>Yes</td>
<td>50 to 90</td>
<td>20 to 40</td>
</tr>
<tr>
<td></td>
<td>QFP with internal spreader</td>
<td>Usually 100 to 240</td>
<td></td>
<td></td>
<td>Yes</td>
<td>20 to 50</td>
<td>15 to 45</td>
</tr>
</tbody>
</table>
Thermal Performance of 100 14x14 LQFP

Larger Flag and Die has better thermal performance. Solid Flag has better thermal performance than X-Flag

Simulations done by Sriram Neelakantan
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Enhancement</th>
<th>Name</th>
<th>Typical i/o Count</th>
<th>Description</th>
<th>Wire Bond?</th>
<th>Theta-JA (1s board) °C/W</th>
<th>Theta-JA (2s2p board) °C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBGA</td>
<td></td>
<td>Plastic Ball Grid Array</td>
<td>16 to 1000</td>
<td>Yes</td>
<td></td>
<td>30 to 90</td>
<td>20 to 50</td>
</tr>
<tr>
<td>TE-PBGA</td>
<td>Thermally Enhanced</td>
<td>Wide range</td>
<td></td>
<td>Four layer substrate with thick planes</td>
<td></td>
<td>20 to 60</td>
<td>15 to 40</td>
</tr>
<tr>
<td>TE-PBGA2</td>
<td>TE-PBGA with internal spreader</td>
<td>Wide range</td>
<td></td>
<td>Internal Spreader</td>
<td>Yes</td>
<td>10 to 20% lower thermal resistance</td>
<td></td>
</tr>
<tr>
<td>TBGA</td>
<td></td>
<td>Tape Ball Grid Array, also fabricated with laminate rather than tape interconnect</td>
<td>Wide range</td>
<td>Die connected to Large Copper Plate</td>
<td>Yes</td>
<td>14 to 20</td>
<td>11 to 15</td>
</tr>
<tr>
<td>FC-PBGA and FC-CBGA</td>
<td>Flip Chip on either ceramic or plastic laminate substrate</td>
<td>Wide range</td>
<td></td>
<td>Flip Chip exposed die vs lid or spreader</td>
<td>No</td>
<td>17 to 50</td>
<td>12 to 25</td>
</tr>
</tbody>
</table>
Typical PBGA (MAP and OMPAC) Thermal Performance

\[ R_{\theta JA} = \frac{T_J - T_A}{P} \Rightarrow P = \frac{T_J - T_A}{R_{\theta JA}} \]

Assumptions: Multilayer application, lots of board area, only low power devices nearby, used junction to ambient thermal resistance on 2s2p test board in natural convection.
Factors in thermal performance:

- **Die Size**
- **Substrate Design**
  - Balls under die – **Don’t depopulate under die**
    - 160 15x15 MAP PBGA 50 °C/W at 36 mm² die to 88 °C/W for 16 mm² Die
  - Vias under die – vias are cheap, use more than 10
  - Metal under the die and bottom side spreader
  - Conductive vs. non-conductive die attach (thickness)
  - Solder Mask Thickness – thin is better
  - Substrate Thickness – thin is better
  - Die thickness for GaAs die

Don’t ask for this design:
No connection from flag to balls
Sample of MAP PBGA Designs

Strong correlation of thermal performance with die size
• Highest power die should be on bottom of stack

• Die attach thermal resistance is 1 to 10 °C/W determined by die size and material

• Choose a ball map which allows ground balls under die with vias through the substrate

• If the DRAM has a maximum temperature rating of 85 °C, it is not a good idea to stack it with other power dissipating components if you have to meet a 85 °C board temperature. Case temperature of 85 °C would be ok.
Package on Package Thermal Test Vehicle

- 604 15x15 MAP PBGA with 7.77x7.77 test die
- Memory (160 15x15 MAP) with 7.77x7.77 test die and 10.4x8.1 spacer die

Junction to Board Thermal Simulation, 0.4 W in bottom die, 0.1 W in top die. Air between packages and between package and board was simulated but not shown for this illustration.

Advantages: Standard memory pinouts, memory die is a little cooler
Heat Sinks Issues
Use Heat Sinks Above 3 W

Use Heat Sinks Above 3 W

Heat Sink $R_{\theta SA}$
Sink to ambient

Interface $R_{\theta CS}$
Case to sink

Package $R_{\theta JC}$
Junction to case

$T_J = T_A + (R_{\theta JC} + R_{\theta CS} + R_{\theta SA})*P$

Theta-JC Determines Whether Heat Sink Useful

Simple View of Heat Sinks assuming all the heat flows to the heat sink
<table>
<thead>
<tr>
<th></th>
<th>Theta-JC Values</th>
<th>Heat Sinks</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBGA</td>
<td>about 5 to 10 C/W</td>
<td>20 to 40% improvement possible</td>
</tr>
<tr>
<td>TBGA</td>
<td>about 2 C/W</td>
<td>dissipate 10 W or more with air flow</td>
</tr>
<tr>
<td>FC exposed die</td>
<td>&lt; .1 C/W</td>
<td>dissipate 70 W instead of 1 W.</td>
</tr>
</tbody>
</table>
Variables

- **Package Internal Resistance** – Theta-JB and Theta-JC depend on die size as well as package size and construction
- **Temperature Range** $T_{j\text{max}} - T_a$ available for cooling, $T_a$ is local ambient to device
- **Radiation** may be more than half the heat flow for natural convection
  - Emissivity of surfaces
  - Temperature of surfaces
- **Air Flow** –
  - Space for natural convection
  - Forced Convection
PBGA, TEPBGA, TEPBGA2

- Theta-JC and Theta-JB are given for customer to create two resistor model.
- Thermal performance for given package size and construction changes with die size.
- For this example, Theta-JC changed 30%.
- Models for Computational Fluid Dynamics (CFD) Simulations are better.
Hand calculation of the heat sink performance will give wrong answer

• Model must consider heat flow path though the heat sink and the heat flow to the printed circuit board.
• Heat flow to the board can be 20% to 75% of the total heat flow.

Recommend attachment of the heat sink to the board

• Clip to substrate not recommended. Bending force by clip on substrate edge can cause early solder joint failures.
Specified heat sinks are not provided because of the range of applications and environments that customers use. Reference heat sinks are sometimes provided to help customers estimate the heat sink requirements.

Example

- Heat sink was designed for CompactPCI board spacing
- Spring clip to plastic frame mounted to board
- Force on heat sink centered over die
FC-PBGA (laminate substrate) with no lid or “die sized lid”

Recommend clip heat sink to board

- Force centered over die (45 newtons maximum)
- Manage warpage of printed circuit board if necessary (Backing Plate)

Glue attachment of heat sink is not recommended (limited area, device not qualified with those forces, die-sized lid uses silicone adhesive with limited peel strength)

Clip to substrate not recommended. Bending force by clip on substrate edge can cause early solder joint failures.
FC-PBGA with Full Footed Lid

Recommend clip heat sink to board

- Force: 45 newtons maximum
- Manage warpage of printed circuit board if necessary (Backing Plate)
TBGA (Cavity Down, heat spreader, wire bond package)

- Thermal interface material must accommodate the fact that the heat spreader (top of package) is not absolutely flat. Recommend considering 0.1 to 0.15 mm variation of interface thickness.
- If heat sink adhesive is used, adhesive must stick to epoxy painted surface.
Thermal Data Usage

• Package Selection

• Determination of test (characterization) temperature requirements

• Calculation of HTOL (High Temperature Operating Life) acceleration factors from junction temperature

• Customer design team needs the data (expects it to be available in datasheet)

• Customer reliability team needs thermal data to validate customer’s design
BACK UP
How fast does it heat?

Calculation of the rate that the die heats in a 604 15x15 POP package. Power is applied to the center 1/3 of the die area. There is no memory package. The package is assumed to be in natural convection on a 100x100 mm printed circuit board with two planes. The heating is calculated to 100 seconds. The die will reach maximum steady state temperature in approximately 3000 seconds.
Flip-Chip Ceramic Ball Grid Array

- Most products for network applications use HiCTE ceramic with a high temperature coefficient of thermal expansion (12 ppm) instead of traditional ceramic with a thermal expansion about 7 ppm. The thermal conductivity of the HiCTE ceramic is only 2 W/m K instead of 16 W/m K of the standard ceramic.

- Recommend clip heat sink to board. Clip to substrate is acceptable for the stiff ceramic substrate, but is not recommended because future devices will probably have laminate substrates.

- Glue attachment of heat sink is not recommended (limited area, device not qualified with those forces)

Note: All current Flip Chip NPI packages are laminate substrate, FC-PBGA