Emerging Trends in Flip Chip

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Flip Chip Growth Drivers

- Flip chip growth of ~25% from 2012 to 2017 in units
  - Microprocessors (all CPUs for PCs)
  - ASICs, FPGAs, and DSPs
  - Chipsets and Graphics
  - Digital TV and other media products
  - Many diodes, filters
- Trends toward copper pillar
- Micro bumps for 3D IC w/ TSV
- Future flip chip growth in wireless products
  - Driven by form factor and performance
  - BB & AP processors moving to flip chip
  - Bottom package in PoP (application processor, many with SnAg bump moving to Cu pillar)

Source: ChipWorks
Apple iPhone5 (side 1)

- SWUA 147 228 is an RF antenna switch module
- Triquint 666083-1229 WCDMA / HSUPA power amplifier / duplexer module for the UMTS band
- Avago AFEM-7813 dual-band LTE B1/B3 PA+FBAR duplexer module
- Skyworks 77491-158 CDMA power amplifier module
- Avago A5613 ACPM-5613 LTE band 13 power amplifier

Source: iFixit
Apple iPhone5 (side 1 continued)

- Qualcomm PM8018 RF power management IC
- Hynix H2JTDG2MBR 128 Gb (16 GB) NAND flash
- Apple 338S1131 dialog power management IC*
- Apple 338S1117 is an unknown device type at this time. The die inside is a Cirrus Logic device (second image) but it does not look like the audio codec.
- STMicroelectronics L3G4200D (AGD5/2235/G8SBI) low-power three-axis gyroscope—same as seen in the iPhone 4S, iPad 2, and other leading smart phones
- Murata 339S0171 Wi-Fi module

Source: iFixit
Apple iPhone5 (side 2)

- STMicroelectronics LIS331DLH (2233/DSH/GFGHA) ultra low-power, high performance, three-axis linear accelerometer
- Texas Instruments 27C245I touch screen SoC
- Broadcom BCM5976 touchscreen controller
- Rather than a single touchscreen controller, Apple went with a multi-chip solution to handle the larger screen size, à la iPad.
- Apple A6 application processor
- Qualcomm MDM9615M LTE modem
- Qualcomm RTR8600 Multi-band/mode RF transceiver, the same one found in the Samsung Galaxy S III

Source: iFixit
Xilinx “Stacked Silicon Interconnect” (2.5D)

- Xilinx 28nm Virtex-7 LX2000T is a 2.5D FPGA solution using a silicon interposer
  - Four FPGA “slices” are co-designed on a 28nm silicon node technology
  - FPGA slices sit side-by-side connected using Amkor’s Cu pillar micro bumps to a passive silicon interposer fabricated with 65nm silicon node technology
  - 50,000 micro bumps per slice, underfilled
  - Silicon interposer contains TSVs with aspect ratio of 10:1
  - Silicon interposer is connected to organic build-up substrate using 19,000 eutectic SnPb bumps and underfilled
- Improved performance
- Lower power
- Xilinx announcement will drive the capacity silicon interposers just as it did for 300mm bumping
- Partnership with TSMC and Amkor provided the infrastructure to support Si interposers
- TSMC will provide future interposer assembly

Source: Xilinx
Bumping Trends: Back to the Future

- Early IBM bump was copper ball
- Early were copper post with solder
  - Citizen Watch
  - Automotive electronics
- Widespread adoption of the high-Pb bump using evaporation process (C4 bump)
  - Licensed and put into production by Motorola, AMD
  - Cross licensing agreement with Intel, but plating process used in production
- Industry moved to electroplated bumps for flip chip
  - Intel
  - TI
  - IBM, Motorola/Freescale Semiconductor, AMD, TSMC
- Industry moving to copper pillar process just as the it transitioned from evaporation to plating
  - Transition started with Intel’s Presler (now all Intel is Cu pillar)
  - TI announced adoption of Cu pillar
  - By 2013-14 move into high volume for many wireless products
  - Many designs moving to Cu pillar at 28nm and beyond

Source: Chipworks.
- Cu plated up with resist mask
- Similar Ti or TiN UBM
- Pb-free solder used on substrate pad (this version)

Source: Chipworks
Why Cu Pillar Flip Chip for CSP?

- Small form factor (smaller die size)
- Finer bump pitch than solder (down to 50 µm)
- Improved electrical performance
- Pb-free solution

Source: Amkor

Source: TI
FC for PoP in Smartphone Application Processors

- TMV PoP for Samsung and Apple smartphones
  - Flip chip in PoP
- Increasing number of examples of application processors with embedded capacitors in package substrate
  - Samsung Exynos with embedded capacitor
- Thinner package and smaller footprint
  - Goal of less than 1.0mm thick packages
  - Flip chip provides improved performance and low profile
  - TMV PoP or PoP with embedded component
  - Future possibility of fan-out WLP on bottom

Source: TPSS
STATS ChipPAC fcCUBE™ Technology

- Ultra high I/O escape routing density
- Scalability to fine bump pitch of 80 microns and finer effective pitch
- Significant reduction of stress on ELK/ULK structures down to 45/50 and 28 nm
- Higher resistance to electro migration
- 20-40% lower cost over standard flip chip for most designs
Unisem’s Cu Pillar

1. Typically the seed layer is a Ti/Cu

2. A photo-imageable resist (either a dry film or spin on) is used to define where Cu will plate up

3. Solder can then be applied through a paste or electroplated process

4. The resist is then stripped, excess seed layer material is etched and then the solder may be reflowed (paste-vs-electroplate)

5. Primary benefits are:
   1. Controlled standoff
   2. Improved electrical performance
   3. Current carrying capability and resistance to electromigration
   4. Thermal dissipation benefits

Source: Unisem

Cu Pillar in HVM for QFNs
Mold compound acts as underfill
ASE Cu Pillar Extended Reliability Test Results

- TV: 65nm, 150µm pitch, die size 5x5mm, pkg. size 10x10mm
- Passed up to HTST3000 (150°C) and TCT3000 (-55 to 125°C)

- TV: 40nm, 162µm pitch, die size 10x10mm, pkg. size 31x31mm
- Passed up to TCT 2500 (-55 to 125°C)

Source: ASE
Flip Chip Assembly: The Bump is Not the Hard Part

- Conventional reflow process with pick-and-place tool
  - Pick, place, reflow, and bond
  - Pitch is limited to around 140 µm, some say 130µm pitch is possible but difficult to do in HVM
  - Underfill is typically capillary flow
- Copper pillar (or column) with solder cap
  - Bump pitch typically ≤140 µm, possible to go to 100 µm and even 40µm staggered bump pitch
  - Most applications are ≤100 µm, but some are 110 or 120 µm
  - Solder cap is typically SnAg, but other alloys possible
  - Some cases capillary flow underfill, but most using non-conductive paste (NCP) and looking at non-conductive film (NCF)
  - Requires high accuracy bonder, but trade-off is slower speed
- Some copper pillar applications are switching to thermo-compression (T/C) bond
  - Underfill material will be non-conductive paste (NCP) or non-conductive film (NCF)
  - Higher precision placement is required, ±2µm accuracy is comfortable for HVM
  - T/C bonders >$1 million, throughput is slower
- Molded underfill considered for some T/C bond applications with ≤30µm bump pitch
  - Especially when a small keep out zone is required, die size is small
Conclusions

• Growth in the use of flip flip packages continues
  – Mobile phones
  – Tablets
  – PCs
  – Telecommunications
  – High-end servers
• Transition in the bump alloy
  – Evaporation
  – Plating
• Today’s transition to copper pillar
  – Many applications
  – Many assembly options