Trends in Test Technology for Advanced Packaging

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TEL Test Systems
The Internet of Things

https://www.youtube.com/watch?feature=player_embedded&v=hz5yOOkTmU8
Honey, I Shrunk the Package?
Package Proliferation

25+ Years of Semiconductor Packaging

Leading edge CMOS node (approx): 0.25um 0.18um 0.13um 90nm 65nm 40nm 28nm


Sophistication & diversification increasing over time

"Backend to the Front Line" William Chen, ASE Group, SWTW 2011
Smart Phone Market Package (Current)

- WLP is majority and increasing its adoption
- FCBGA (incl. POP) is used for high pin counts and large die

Graph showing chip size vs. PKG ball count for smartphone and tablet devices. Key points:

- WLP (including FCBGA and POP) availability
- Ball Pitch: 0.4mm

Source: TEL MKT

Galaxy S4, iPhone5, Coolpad, Ascend D2, iPad mini, UMI X1S

Major Smart Phone Device & Package:
- AP
- CIS
- BB
- Touch Control
- WiFi Combo
- Panel Driver
- RF TRX
- PMIC
- Power AMP
- Sensor
- NAND
- DRAM
2. 3D Test Flow

2D Test Flow vs. 3D Test Flow

Conventional 2D

- wafer fab
- wafer test
- assembly & packaging
- final test

3D-SIC

- wafer fab 1
- wafer fab 2
- ... wafer fab n
- KGD test 1
- KGD test 2
- ... KGD test n
- stacking 1+2
- stacking (1+2)+...
- stacking (1+2+...)+n
- KGS test 1+2
- KGS test (1+2)+...
- KGS test (1+2+...)+n
- assembly & packaging
- final test

- Ruled by same benefit-cost equation: \((1-y) \cdot d \cdot p > t\)
  - \(p\) : more comprehensive; not just package, but also other dies
  - \(y, d, t\) : what faults are we targeting in KGD/KGS test?
Test for WLP

Standard Package Test Process

1. Wafer Process
2. Wafer Test
3. Dicing & Assembly
4. PKG Test
5. Ship

Packaged at Wafer Level

WL-CSP Test Process

1. Wafer Process
2. RDL Bumping
3. Wafer Test
4. Dicing
5. Ship

Not Check Dicing defect

1. Wafer Process
2. RDL Bumping
3. Dicing
4. Wafer Test
5. Ship

Able to check Dicing defect

Able to check Dicing defect

Std Wafer Prober

Dicing Frame Prober
# Test System / Product Line

**Wafer Prober**

*Model: Precio™, XL*

**Application**
- Regular Wafer: 8, 12inch
- Memory, Logic
- 3D Integration Device

**Feature**
- High Accuracy (XY: ±1.8um)
- High Productivity
- High Through-put
- Small Footprint
- Short Lead Time

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**Dicing Frame Prober**

*Model: WDF™ 12DP+

**Application**
- Regular Wafer: 8, 12inch
- Dicing Frame: 12inch, 8inch*
- Memory, Logic
- 3D Integration Device, KGD
- RMA

**Feature**
- High Contact Accuracy
- High Productivity/Through-put
- Partial map auto recognition for RMA
Tutorial on Frame Probing
What changes in the Wafer Test Process when probing thinned or diced wafers →

- Operators are skilled at handling Standard Wafers
- Wafer edge is clear and identifiable
- Die are Perfectly Aligned
- Perfectly reproduced / repeated die lay out

CSP Wafer (InFO-WLCSP, EWLB)
CSP Test – Un-Diced / Thinned Wafers

Operators are required to handle frames

Completely different:
- Product Shape
- Way to handle
- Type of cassette
- OCR / Bar code System

This is in the case of un-diced wafers
CSP Test - Diced wafers

For wafer that are diced →

Variables:
- Product Shape
- Way to handle
- Type of cassette
- OCR / Bar code System
- Die position
- Wafer edge undefined

Imperfect / Variable die position
CSP Test – Things to watch for

- Wafer position on the frame
  - It can be rejected by the prober
    - At pre alignment stage
    - At Wafer edge recognition

- How to prevent?
  - Proper setup on the frame / wafer positioning machine
CSP Test – Things to watch for

Sag on the Film:
- Can happen after extended storage
- Stored without Humidity / $T^\circ$ controlled environment

 Risks?
- Pincette not able to pickup the Frame.
- Die miss aligned once on the chuck

 How to prevent?
- Good & consistent film quality
- Good setup on the Frame / Wafer positioning machine
- Good storage conditions
CSP Test – Things to watch for

Warp Frame:
- Can happen if the frame quality is poor
- If it has been recycled without proper quality checks

Risks?
- Sticking in the cassette
- Pincette damage/break
- Prober not able to handle it
- Interrupt for Operator assist

How to prevent?
- Good & consistent quality check for new and recycled frame
CSP Test – Quality of the probing

Any impact?

Probing is same as standard wafers:
- Same edge recognition / Wafer alignment
- Position of the wafer on the film is key
- Good bar code positioning important
- Handling speed slightly reduced

Probing will be same as standard wafers if:
- Dicing quality is constant
- Film is stable in time
- Storing packing conditions are stable
- If required the N Shot alignment function is used
WDF12DP+

New 300mm Dicing Frame Prober
WDF12DP+ Feature

• 12inch and 8inch Frame and Wafer handling
  – Standard: 12inch
    • 12inch Dicing Frame
    • 8inch and 12inch Wafer
  – 8inch COK
    • 8inch Dicing Frame
    • 8inch Wafer

• TEL Standard software “PSAS
• Software compatibility
• Combo480SQ interface
• Auto partial map recognition
Partial Map/Option

Special software feature/option for the demand of RMA purpose to test diced die or PKG which are deployed in partial area of Dicing Frame. WDF12DP+ can automatically recognize test area without operator interaction.

Current Test Flow

“Normal Test flow” + “Broken Wafer mode for Last wafer”

WDF12DP+ Flow

“Normal Test flow” + “Auto(Partial Map)”
FOWLP Test Challenges

Std Wafer

CSP Wafer (InFO-WLCSP, EWLB)

Due to wafer reconstitution in mold compound and CTE during thermal, planarity of wafer renders chuck vacuum challenges: initial chucking and maintaining vacuum during probing.
### Implemented Solutions

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<thead>
<tr>
<th>Chuck TOP</th>
<th>Vacuum</th>
<th>Handling Arm1</th>
<th>Power Assist</th>
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</thead>
<tbody>
<tr>
<td>New Chuck (FOWLP Type)</td>
<td>New vacuum line Sequence</td>
<td>Modified Pad Type</td>
<td>Air Pusher</td>
</tr>
<tr>
<td>Additional Vac Line</td>
<td>phased vacuum sequence from center</td>
<td></td>
<td></td>
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</tbody>
</table>

**Under Development**

- Air Pusher
Wafer Level System Level Test Probing
Precio SLT System
Summary

• Packaging continue to Shrink
• Testing methods are adapting to the Package Shrink and Chip Bundling
• The Key to the future of Semiconductor Testing is Package Handling