A Review of Semiconductor Packaging .......an industrial perspective

...can we apply any of this to HB LED packaging??

Gerry Keller
Consultant
Madera Solutions LLC
Abstract

One of the biggest limitations for LED penetration of the lighting market is product cost.

This presentation looks at the evolution of packaging and industrialization in semiconductors from its early days until today and analyzes the driving forces that have influenced that evolution.

It asks the questions 1) what can we learn from semiconductor packaging and 2) what can we leverage from semiconductor packaging and industrialization and apply to HB LEDs.
Package Evolution Over the Years

- Transistor Outline (TO) “metal cans”
- Dual Inline Package (DIP) CERDIP / PDIP
- Small Outline (SO) SOT / SOIC / TSSOP
- Quad Flat Package (QFP)
- Quad Flat No-leads (QFN) Multi-row QFN / TQFN
- Plastic Leaded Chip Carrier (PLCC)
- Ball Grid Array (BGA) CBGA / PBGA / FPBGA
- Stacked BGA Flip Chip/Wire Interconnect

1950 - 2013
LED Package Evolution Over the Years

- **1950s**: TO-92 Plastic Pkg
- **1970s**: TO-92 Plastic Pkg, Rebel – SM (C), Backlight – SM (P), Multi Die – SM (C)
- **2010s**: Surface Mount (P), Rebel – SM (C), COB – IMS, 1 mm sq, CSP – SM (S)

Package Types:
- Dual Inline Package (DIP)
- CERDIP / PDIP
- Small Outline (SO)
- SOT / SOIC / TSSOP
- Plastic Leaded Chip Carrier (PLCC)
- Quad Flat Package (QFP)
- Quad Flat No-Leads (QFN)
- Multi-Row QFN / TQFN
- Stacked BGA

 Technologies:
- Flip Chip/Wire Interconnect
- Ball Grid Array (BGA)
- CBGA / PBGA / FPBGA
- WLCSP
Packaging Evolution (first wave)

Thru Hole Technology

- Typically single unit at time (assembly jigs)
  - Easy for the end user (manual assembly)
    - Lead Pitch at 2.50 mm or greater
    - Transitioned to lower cost plastic encapsulation
      - Lead frame handling and early automation

20 Years
Characteristics of the First Wave

- Several Major Semicon Companies
  - OEM Equipment Development Teams
  - OEM Packaging Development Teams
  - Vertically integrated in many cases (own lead frames and other materials)
  - Many silos to work from (a diversity of ideas/concepts)
  - Immaturity – nothing worked quite as it was expected to…
  - General dissatisfaction with quality/effectiveness

- Solutions came from many suppliers
  - Companies quick to try new ideas
  - Much diversity within a given company/factory
  - Need to clean-up, standardize became apparent
  - Remote solutions. Factory in one location, Development in another
Material Handling in Equipment

Lead Frame Evolution

- Dedicated by Package size
  - Hence Equipment dedicated
  - Flexible equipment was not effective!
  - Not readily re-useable

- Tooling Up Cost substantial for a new package
  - Capex Intensive
  - Tooling Intensive
  - High Cost/Unit
  - Long Lead Times
Material Handling in Equipment

Early Efforts in Flexibility
- Somewhat effective in Flexibility
  - But quite wasteful on material usage
- Okay for low volume
- Started wheels turning on more flexible approaches
Packaging Evolution (second wave)

Surface Mount Technology

Standardization

Process Capability & Quality

Surface Mounts on Cu Substrates

BGA Substrates

- Surface Mount Technology packaging evolved
- Board Mounting technologies for Surface Mounts improved rapidly
- New Equipment required w/more Automation and Better Quality
- Smaller Pitch 1.25 mm (1.50mm for BGA)
- Matrix Lead frames (multi-rows)

Engaging Supplier Base

Factories Beginning to lead Effort
Packages and Beliefs Changing

Encapsulate Utilization improved Radically over time
- More Impressive when viewed by usage per I/O
- improved significantly from a system standpoint (material usage, waste, transportation cost, recycle costs)

Courtesy of Amkor Semiconductor
Map Array molding and saw singulation were pioneered on BGA

- Map Array Matrix Lead frames significantly improved cost of BGAs
- Solved some quality issues around molding on FRP

Matrix Lead Frames → Map Array Substrates

- Map array molding introduced with BGAs
  - High Tooling cost cycle broken with BGA & later QFN!
    - Mold cavity simplified and standardized with Map Array
  - QFN Map array products introduced
    - Half-Etch approach critical to QFN quality
    - With high density, Etched L/F competitive with Stamped
    - Trim and Form tooling eliminated, moved to sawing
    - Simplification, Materials Utilization, Low Cost
Comparing Cost and Cycle Time

### Comparing Individual Cavity vs Map Array Packages

<table>
<thead>
<tr>
<th>Major Tooling</th>
<th>Individual Package Molding</th>
<th>Map Array Molding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tooling</td>
<td>Leadtime</td>
</tr>
<tr>
<td>Leadframe</td>
<td>Stamped</td>
<td>10-14 weeks</td>
</tr>
<tr>
<td>Package Cavity Molds</td>
<td>Cavity Mold</td>
<td>10-14 weeks</td>
</tr>
<tr>
<td>Singulation</td>
<td>Trim/Form</td>
<td>10-14 weeks</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>New Product Development</th>
<th>Individual Package Molding</th>
<th>Map Array Molding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>Leadtime Dependent</td>
<td>Short -- Depending on Map Mold</td>
</tr>
<tr>
<td>Cost</td>
<td>High Tooling Costs</td>
<td>Low - Very Little Hard Tooling</td>
</tr>
<tr>
<td>Ability to Iterate Rapidly</td>
<td>Cost and Cycle Time</td>
<td>Low Cost / Fast Turn Around</td>
</tr>
</tbody>
</table>

Many advantages to Map Array molding vs Individual Cavity. Not only is the initial product release much faster, the initial investment is much lower. The sustaining cost on not having to maintain extensive tooling reduces overall operating costs.
Many Subtleties – Map Array vs Cavity

Clamping Force required to control Resin Bleed

SOIC-8 / 224 units per lead frame
Package Perimeter = ~18 mm
Total Perimeter of Leadframe clamping = ~4000 mm

SOIC would require >200 ton press

Map Array would require only ~ 50 ton press

QFN-16ld / 1500 units per lead frame
Total Perimeter = 630 mm or <20% of cavity leadframe equivalent
Highly Structured Industrialization

- High Density Lead Frames and Substrates Standardized
  - Map array molding Leveraged in QFN
    - Material Utilization (pitch shrink, package thickness, HD arrays)
      - Noble Metals challenged (Cu wire, smaller wire)
      - Usage optimized (metal thickness, metal stacks, resins)
      - Process Simplification (fewer steps, less material)
        - Systems Approach (total cost)
# Impact of Package Lead Pitch

## Amkor Package Capability vs. PBGA & SuperFC Products

<table>
<thead>
<tr>
<th>Package Type &amp; Body Size</th>
<th>PBGA 0.8mm</th>
<th>Leadcount and Pitch</th>
<th>PBGA 1.0mm</th>
<th>Leadcount and Pitch</th>
<th>PBGA 1.27mm</th>
<th>Leadcount and Pitch</th>
<th>Factory</th>
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<tr>
<td>19.0 x 19.0</td>
<td>529</td>
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<td>324</td>
<td></td>
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<td>P3, K4</td>
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<td>21.0 x 21.0</td>
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<td></td>
<td></td>
<td>P3, K4</td>
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<td>23.0 x 23.0</td>
<td>484</td>
<td></td>
<td>289</td>
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<td>P3, K4</td>
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<td>729</td>
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<table>
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<th>SuperFC®</th>
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<td>K4</td>
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<td>[2912]</td>
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</table>

4X Improvement in same footprint!

Courtesy: Amkor Semiconductor
Package Size vs I/O count

- PDIP
- TSSOP
- SOIC
- QFP
- QFN
- Dual row QFN
- BGA

- PDIP-64 900 mil
- SOIC-32 300 mil
- TSSOP
- QFN
- 2-row QFN 12 x 12 mm 156-164 leads
- WLCSP (estimate)

- TQFP 28 x 28 mm 256 leads
- BGA 23 x 23 mm 1156 leads
Major Semiconductor Package Trends

IC SHIPMENT BY PACKAGE CATEGORY

- Flip Chip (DCA, WLP)
- Flip Chip in Package
- Array Package (BGA, CSP, PGA)
- Modified Leadframe (QFN, MLF)
- Surface Mount (SO, QFP)
- Through Hole Bare Die (COB)

Source: Prismark Partners LLC, Presentation on Advanced Packaging Trends, July 2003

QFN is the fastest growing package in the industry!
Source: Reconstructed from Prismark 2Q’14 Report
Actual SOT 23 Cost Learning Curve

Major Mature Product
(specific factory)

LC for a +30 yr old package

$60/K 1980

1992

1998

2004

$0

2002 Industry Benchmark (3$/K units)

2000-01 Recession exposed huge cost gap

70% Learning Curve

Actual Learning Curve 63.3% over 12 years
There is enough industry data that you can bet on the learning curve. The LC is based volume. Without incremental volume limited improvement!
Sustainability Summary

Engineered Reductions

- Au Wire 39% Save
- Footprint 92% Reduction
- Compound 93% Save
- Leadframe 97% Save

Same Device functions packaged more efficiently

Index

Time

Integrating Technological Requirements for Industrialization

75% Semiconductor
- Experience Curve
- Supply Chain
  - Materials
  - Equipment
  - CMs
- Volume
- Quality
- Infrastructure

25% HB LED
- Extraction Efficiency
- LED Specific Material Needs
  - Reliability Requirements
  - Optical Needs
  - Thermal Needs
- Bridging to Semi Equipment

Leverage

Incorporate
# Comparing Semicon and COB Process Flows

<table>
<thead>
<tr>
<th>Process</th>
<th>Equipment</th>
<th>Semicon</th>
<th>LED COB</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matl Handling</td>
<td>Magazines for Transport</td>
<td>Yes</td>
<td>Yes</td>
<td>Same Standard Magazines</td>
</tr>
<tr>
<td>Die Prep</td>
<td>Die Saw</td>
<td>Yes</td>
<td>n/a</td>
<td>Sorted Die on Film Frames</td>
</tr>
<tr>
<td>Substrate Clean</td>
<td>Plasma Clean</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Die Attach</td>
<td>Die Attach M/C</td>
<td>Yes</td>
<td>Yes</td>
<td>Conductive epoxy</td>
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<tr>
<td>Wire Bond</td>
<td>Wire Bond M/C</td>
<td>Yes</td>
<td>Yes</td>
<td>Au Wire 25um</td>
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<tr>
<td>Molding</td>
<td>Auto Mold System</td>
<td>Yes</td>
<td>n/a</td>
<td></td>
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<tr>
<td>Dam Dispense</td>
<td>Precision Dispense</td>
<td>n/a</td>
<td>Yes</td>
<td>Dispense with snap cure</td>
</tr>
<tr>
<td>Phosphor Dispense</td>
<td>Precision Dispense/Degas/Cure</td>
<td>n/a</td>
<td>Yes</td>
<td>Integrated Degas and Cure</td>
</tr>
<tr>
<td>Full Cure</td>
<td>Oven</td>
<td>Yes</td>
<td>Yes</td>
<td>Std equipment for cure processes</td>
</tr>
<tr>
<td>Mark</td>
<td>Laser Mark</td>
<td>Yes</td>
<td>n/a</td>
<td>Integrated with test for LEDs</td>
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<tr>
<td>Test &amp; Mark</td>
<td>Custom LED Test &amp; Mark</td>
<td>n/a</td>
<td>Yes</td>
<td>Test and Mark with lot and part specifics</td>
</tr>
<tr>
<td>Singulate and Sort</td>
<td>Std Semicon package Saw</td>
<td>Yes</td>
<td>Yes</td>
<td>Added 2D reader for Sorting</td>
</tr>
<tr>
<td>Test</td>
<td>Pick and Place Test</td>
<td>Yes</td>
<td>n/a</td>
<td></td>
</tr>
<tr>
<td>Pack</td>
<td>Std JEDEC Trays w/specific Cavity</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>

Leverage existing Semiconductor equipment wherever possible. Use highly professional equipment integrators to fill the gaps for mag to mag processing.
What a Journey!!!

From this!

To this!
Semicon........a $400 Billion/Yr Industry
Leverage.... *this Powerful Engine*

Can HB LEDs ride in the slipstream of Semiconductors
Appendix
Why BGAs are so Popular

<table>
<thead>
<tr>
<th>CABGA Package Thickness Offering</th>
</tr>
</thead>
<tbody>
<tr>
<td>CA-lFBGA</td>
</tr>
<tr>
<td>CA-lFBGA-CBGSA/CAS0N</td>
</tr>
<tr>
<td>CA-lFBGA-CVBGA/CAS0N</td>
</tr>
<tr>
<td>CA-wFLGA</td>
</tr>
<tr>
<td>CA-wFLGA-CAS0N</td>
</tr>
<tr>
<td>CA-xFLGA</td>
</tr>
<tr>
<td>CA-xFLGA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package Thickness</th>
<th>&gt; 1.2mm</th>
<th>1.2mm (max.)</th>
<th>1.0mm (max.)</th>
<th>0.8mm (max.)</th>
<th>0.65mm (max.)</th>
<th>0.50mm (max.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Layer</td>
<td>2lyr</td>
<td>2ly or 4ly</td>
<td>2ly or 4ly</td>
<td>2lyr</td>
<td>2lyr</td>
<td>2lyr</td>
</tr>
<tr>
<td></td>
<td>0.32 mm, 0.56 mm</td>
<td>0.21 mm, 0.26 mm</td>
<td>0.21 mm</td>
<td>0.21 mm, 0.13 mm</td>
<td>0.13 mm</td>
<td>0.13 mm</td>
</tr>
<tr>
<td></td>
<td>4ly or 6ly</td>
<td>0.34 mm, 0.56 mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max Die Thickness</td>
<td>0.27 mm</td>
<td>0.23 mm</td>
<td>0.18 mm</td>
<td>0.13 mm</td>
<td>0.10 mm</td>
<td>0.075 mm</td>
</tr>
<tr>
<td>JEDEC Name</td>
<td>LFBGA</td>
<td>TFBGA</td>
<td>VFBGA</td>
<td>WFBGA</td>
<td>UFBGA</td>
<td>XFBGA</td>
</tr>
</tbody>
</table>

LGA options are available with screen printed bumps. Die thickness is also dependent on the wire loop height requirement.
**LED Packing Density**

<table>
<thead>
<tr>
<th>LED Type</th>
<th>T-Pack</th>
<th>Surface Mount</th>
<th>Chip on Board</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Image</strong></td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td><strong>Packed Array (10mm x 10mm)</strong></td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>9 LEDs</td>
<td>40 LEDs</td>
<td>342 LEDs</td>
</tr>
<tr>
<td><strong>Array Power</strong></td>
<td>0.4 Watts</td>
<td>4 Watts</td>
<td>68 Watts</td>
</tr>
</tbody>
</table>

WLCSP LED emitters could be a lower cost and more flexible alternative to COB while approaching COB densities.
Presenter Background

- Started as an Industrial Engineer (electronics assembly)
- Manufacturing Engineer (computer manufacturing)
- Production Management (semiconductor test)
- Operations Management (semiconductor assembly/test)
- Rationalization Management (capacity, capex & package engineering)
- Factory Gen. Management (semiconductor assembly/test)
- Global Competence Management (semiconductor package and equipment development, strategy and contract manufacturing)
- NPI (Support New Product Development Team) (HB LEDS)
- Industrialization of New Products (HB LEDS)
Gerry Keller Bio

Gerry Keller has been consulting for the last 7 years mostly with LED lighting companies (start-up and established). His focus has been new product Introduction (NPI) with DFM and industrialization focus for those products. Activities including identification and selection of contract manufacturers and bringing product to full production with the CMs. He has also worked with companies on Cost Reduction strategies/programs and Quality trouble shooting.

Prior to that he had various positions with Motorola and Philips semiconductor assembly and test operations both domestically and internationally. He started as a production manager, later operations manager and factory general manager. He also led engineering teams with worldwide responsibility for package development and industrialization. He spent more than 12 years living and working in Asia and traveled extensively in the region to engage equipment and materials suppliers as well as contract manufacturers. This has enabled him to develop a significant network of suppliers, that have proved very helpful in his consulting work.

Early in his career he worked as an industrial engineer in various industries and as a manufacturing engineer in the computer industry. Experiences gained in those hands-on assignments have helped to build a strong foundation for a future in operations and engineering management. Gerry is a strong disciple of TQM, 6-Sigma, TPM and operational excellence and has a established track record built on those disciplines.

Gerry received a BBA in Industrial Management from the University of Texas and an MBA from Texas State University with a focus on management.