Embedded Package Technologies
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- SESUB – Overview
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Package Interconnect Evolution

- Embedding thin chips into substrate build-up layers by using well-established substrate technology.

- Electrical contacts to the chips are realized by laser-drilled and metallized microvias.
Die Embedding Applications & Options

- **Substrate Based Embedding**
  - Driver - Size/Performance

- **Hybrid Substrate/Lead-frame Embedding**
  - Driver - Power/Thermal/Performance

- **Fan Out Based Embedding (Chip First/Last)**
  - Driver - Die Size/Performance
Power Packaging Examples

**uPower Module**
- BGA / LGA Module
- Embedded Inductor & Capacitors (<40V, <10A)
  - (e.g. Step-Down, Buck-Boost, LED Drivers & Battery Chargers)

**Mid-Power Module**
- Mid-Power Modules with Cu-clip & Al wedge bond
- DIP (Dual In-line PKG) IPM
- Multi-chip modules (<220V, <20A)
  - for AC/DC converter in white goods, Industrial motors Etc.

**IPM & SMPS**
- IPM : Intelligent Power Module
- SMPS : Switching Mode Power Supply
- Multi-chip as IGBT + Diode + HVIC + LVIC (<600V, <30A)
  - for AC/DC converter in white goods, Industrial motors Etc.

**IGBT Housing Module**
- Housing Module
- High Reliability / High Power Module
  - (600V~1200V / 1200V~3500V, Upto 100Kw)
  - DC/DC Converter / DC-AC Inverter in automotive, (H)EV, Power Train etc.
Benefits of Embedded Packaging

- **Miniaturization & Design Flexibility**
  - Embedded chip enables more space for other components or shrinks overall solution
  - Design flexibility now shifts from 2D to 3D

- **Improved Thermal & Electrical Thermal Performance**
  - Shorter interconnections reduce parasitics - minimizes distortion and power loss
  - Lower electrical & thermal resistivity in package improves power performance

- **Improved Reliability and mechanical stability**
  - High mechanical system stability due to stable Cu interconnections.
Electrical Considerations of Embedding

Embedded Packaging Reduces Parasitics Through:
- Shorter Connections (Example - Wire Bond Elimination)
- Shorter Distance Between Components- Passives closer to Chip Pads
- Fewer Capacitance Areas
Understanding Ohms Law for Packaging

- Ohm’s Law - Power Loss = Current Squared x Resistance (Double the Current give you 4x the Power Loss)

- Physical Explanation – The voltage difference along a wire depends on the current – More current flowing with resistance mean more voltage (pressure of electricity if you like) is built up.

- Practical Explanation – Power measured in watts is equal to I x R along the path of circuit. If you keep resistance small, you minimize power loss as HEAT!!

**Physics Forum 2008**
Overview - Embedded Package Solutions

SESUB - Semiconductor Embedded In Substrate

aEASI – Advanced Embedded Active System Integration
SESUB – Semiconductor Embedded in Substrate
What’s **SESUB**?

SESUB = Semiconductor Embedded in SUBstrate

- ASE offer SESUB by the JV with TDK.
- IC wafer grinded to 50um (min.) and embedding in resin substrate.
- Total substrate thickness 300um and below.
- SESUB is already proven technology by many customers and IC vendors.
Product Portfolio Examples

**SESUB (Semiconductor Embedded in SUBstrate)**

- 4 Metal layers
- Total thickness: 300 um typically
- Core thickness: 115 um typically
- Die thickness: 50um min.
- IC ratio (die/substrate): 15 ~70%
- Production: Available
- (Max 12x12 mm² size experienced)

**S-SESUB (Simplified Semiconductor Embedded in SUBstrate)**

- 2 Metal layers / Cavity Core
- Total thickness: 250um typically
- Core thickness: 160 um typically
- Die thickness: 100um Typically
- IC ratio (die/substrate): 30% max.
- Production: Available
**SESUB** Key Features

### PCB Miniaturization

- **COB Solution**
  - Die: 8.5x8.5x1.4mm, 73mm²
  - PCB: 13.0x16.5mm, 215mm²

- **SESUB Module**
  - Die: 5.6x4.0x1.0mm, 26mm²
  - PCB: 11.5x11.5mm, 132mm²

Embedding IC releases surface space for other components, or allows reduction of the overall substrate size.

### Better Heat Dissipating

- **PKG Surface**: 54 °C
  - **Junction**: 63 °C

- **Heat Dissipating**: -9 °C

Short Cu Connections reduce parasitic and lead minimum signal distortions, better heat releasing by design.

### Mechanical Robustness

- **Wiblok Plot for Dropping**

Trace pattern and Embedded IC chip allows high mechanical system stability with highly reliable Copper Interconnections, no wire bonding nor soldering.

### Improving Performance

- **System IC**
  - **Signal Line**
  - **Memory IC**

Short Cu Connections improve parasitic and lead minimum signal distortions, better heat releasing by design.
Application Space for SESUB – Some Examples
aEASI – Power Embedding
What’s \textit{a-EASI}?

\textbf{aEASI} = \textit{Advanced Embedded Active System Integration}

- Leverages a Mature Organic Substrate Process Flow Modified to Meet High Power Applications
- Good Current Capability- \( \sim 60\text{A} \) (Integrated Power Stage Example), \( \sim 1.9\text{W/mm}^2 \)
- 300um thick Copper Heat Spreader/Electrical Pad (Back of Die)
- Copper Lines \( \sim 32\text{um} \) Thick for Low Resistivity
- Deep Full Filled Vias to Die \( \sim 130\text{um} \) Diam
- Ultra Low Resistivity Die Attach Interface
aEASI Product Examples

aEASI P1 structure
Package Size: 5 x 5 x 0.57 mm (exclude passives height)
1 Micro Power Management Chip
Passives: 12pc
0806 x 2, 0603 x 2, 0402 x 4, 0201 x 4
RDL: 2+1 Layer

aEASI P1 structure
Package Size: 6.65 x 4.55 x 0.8 mm
2 power MOSFET + 1 Driver
RDL: 2+1 Layer
aEASI Package Portfolio

**P1**
- Passive/Active integrate on top is possible
- Smaller Package Footprint
- BGA/LGA foot print

**P2**
- Passive/Active integrate on top is possible
- Cavity lead frame – Better process control
- QFN/BGA/LGA foot print
- Superior thermal performance (exposed pad)

**P3**
- Passive/Active integrate on top is possible
- Dual side cavity lead frame – Better design flexibility for vertical current devices or multiple die
- Support Stack die configuration
- BGA/LGA foot print
A-EASI Example Cross Section – Integrated Power Stage

- Thick Cu (32µm)
- Small via (Diameter = 70µm)
- Deep Via (aspect ratio ~1.1)
- Via on Die pad (50µm min in Via bottom)
- Thin Die (~50µm)
aEASI Package to Die Interconnect Highlights

- Design for power devices

- Thick Cu RDL (32 um). Minimize turn on resistance.

- Prepreg material provide >2.5KV breakdown voltage

- 50um via diameter (Equal to 4 x 1 mil wire bond in conductor area)

- Cu to Cu interface. Minimize reliability risk in high current density condition

Chip Cu Pad
## Reliability Test (P1 Structure)

* P2/P3 under development

<table>
<thead>
<tr>
<th>Test description</th>
<th>Abbr.</th>
<th>Condition</th>
<th>Readout</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Conditioning J-STD-020D</td>
<td>PC</td>
<td>MSL3, 3x260°C, Reflow</td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Biased Highly Accelerated Stress Test JESD22 A110</td>
<td>HAST</td>
<td>Ta = 130°C RF = 85%</td>
<td>0 h precon 96 h</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling JESD22 A104</td>
<td>TC</td>
<td>T min = - 55°C T max = 150°C tt = 5s</td>
<td>0 c precon 5000 c 10000 c</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Storage Life JESD22 A103</td>
<td>HTSL</td>
<td>Ta = 150°C</td>
<td>0 h precon 168 h 500 h 1000 h</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Operating Life JESD22 A108</td>
<td>HTOL</td>
<td>Ta = 125°C Tj = 150°C</td>
<td>0 h precon 168 h 500 h 1000 h</td>
<td>Pass</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Power Temperature Cycling JESD22 A105</td>
<td>PTC</td>
<td>T min = - 40°C T max = 125°C</td>
<td>0 c precon 5000 c 10000 c</td>
<td>Pass</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pass</td>
</tr>
</tbody>
</table>
aEASI P2

Ag Sintering

Passives

Bottom View
## P2 BGA Reliability Summary

**Key information:**
- **Size:** 4.0x4.0 +/- 0.1 mm, **TH** = 0.35 +/- 0.040 mm
- **Ball count:** 24 (pitch: 0.5 mm)
- **Blind Via:** 0.085 mm
- **T/S:** 60/60
- **Cavity lead frame**

### Test Description

<table>
<thead>
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<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preconditioning AEC-Q100</td>
<td>PC*</td>
<td>MSL3 MSL Moisture soaking3 30°C/60%RH</td>
<td>Bake 125°C 24Hrs Moisture Soak 168 Hrs 3x Reflow (265°C+(0/-5))</td>
<td>Pass</td>
</tr>
<tr>
<td>HAST AEC-Q100</td>
<td>HAST</td>
<td>130°C/85%RH 33.3PSIA</td>
<td>100hrs</td>
<td>Pass</td>
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<tr>
<td>Temperature Cycling AEC-Q100 Grade 0</td>
<td>TCT</td>
<td>“-65”~150°C</td>
<td>500 Cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>HTST AEC-Q100 Grade 0</td>
<td>HTST</td>
<td>150°C</td>
<td>500 hrs</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000hrs</td>
<td>Pass</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>1500hrs</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2000hrs</td>
<td>Pass</td>
</tr>
</tbody>
</table>

The diagram shows the top and bottom views of the BGA component with dimensions 4.0 mm x 4.0 mm.
P2 QFN

Key information:
- **Size**: 5.0X 5.0 +/- 0.1 mm, TH = 0.305 +/- 0.040 mm
- **Lead count**: 20 Pin (Lead pitch: 0.735/0.8mm)
- **Blind Via**: 0.06 mm
- **T/S**: 40/40
- **Laser marking on SM**: Passive/Active integrate on top is possible

<table>
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<th>Condition</th>
<th>Readout</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preconditioning</td>
<td>J-A113/0-020</td>
<td>JESD22-118</td>
<td>PC* MSL3 Moisture soaking3 30°C/60%RH</td>
<td>Pass</td>
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<tr>
<td>HAST</td>
<td>J-ESDD22-A118</td>
<td>HAST</td>
<td>130°C/85%RH 33.3PSIA</td>
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<td>Temperature Cycling</td>
<td>JESD22-A104</td>
<td>TCT</td>
<td><del>-65</del>150°C</td>
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</tr>
<tr>
<td>HTST</td>
<td>JESD22-A103-B</td>
<td>HTST</td>
<td>150°C</td>
<td></td>
</tr>
</tbody>
</table>
Electrical Performance Comparison

![Resistance Graph](image)

![Power Efficiency Graph](image)

- Resistance comparison:
  - PQFN (Cu clip): 15.00 mohm
  - PQFN (Cu wire): 34.15 mohm
  - aEASI - P1: 0.59 mohm
  - aEASI - P2: 0.56 mohm

- Power Efficiency:
  - OFN
  - aEASI

Output Current (A): 0 to 50
Power Efficiency (%): 60% to 100%
Thermal Performance

<table>
<thead>
<tr>
<th>Component</th>
<th>Thickness</th>
<th>Theta JA (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PQFN (Cu Clip)</td>
<td>6x6 mm</td>
<td>32</td>
</tr>
<tr>
<td>PQFN (WireBond)</td>
<td>6x6 mm</td>
<td>33</td>
</tr>
<tr>
<td>aEASI - P1</td>
<td>6.5x4.5 mm</td>
<td>31</td>
</tr>
<tr>
<td>aEASI - P2</td>
<td>6.5x4.5 mm</td>
<td>29</td>
</tr>
</tbody>
</table>
Summary

- Packaging interconnect technology has evolved and for the next level of minaturization and performance enhancement, embedded packaging will be a key enabler.

- Bluetooth/Wifi modules, Power Analog Devices and new SiP Modules are leveraging this technology to enable better size, electrical and thermal performance.

- Embedding Package solutions such as SESUB and aEASI are available embedding solutions that have proven benefits for low and high power analog, digital and RF products.

- ASE is the leader in System in Package/System in Module packaging and embedding package technology is a key tool to further enable the next generation of high performance products.
Innovative IC, System-in-Package, and MEMS packaging portfolio for today’s miniaturization, mobility, and IoT needs.

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