The Future of Packaging and Assembly Technology

- Track Innovation
- Identify Trends
- Analyze Growth
- Influence Decisions

Relevant, Accurate, Timely

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Outline

- Industry Trends
- Flip chip developments
- WLP developments
  - Fan-in WLP
  - FO-WLP as a disruptive technology
- SiP: Many different packages
- Trends in 3D IC and silicon interposers
Industry Trends 2016: A Few Observations....

- Industry is in an unprecedented “era of change” as our industry matures
  - Trend in mergers and acquisitions will continue this year
  - This year will be a “strange” year
- PC industry unit volumes remain flat
- Despite IoT “hype” mobile devices such as smartphones still driving unit volumes in semiconductor industry
- Thin products are driving thin package solutions
  - Must meet steep ramp with high volume
- Trend in WLP use for mobile products such as smartphones continues
  - Conventional WLP
  - FO-WLP
- Growth in the use of flip chip packages continues, with quest for lower cost solutions
- Wire bond still workhorse of industry, but higher growth rates in FC and WLP
- Moore’s Law proving more difficult to maintain
  - Next technology nodes become more expensive
  - Rely on semiconductor packaging to achieve lower system cost
  - Driving multi-die and system-in-package (SiP) solutions
- The road ahead requires new developments to lower packaging cost
  - Adoption of new technologies to achieve cost/performance trade-off
Major Growth Drivers in Electronics Industry

Computing Growth Drivers Over Time, 1960-2020E

- Today’s driver mobile phones
- Industry perception that future growth driven by “connectivity”
- Cisco calls it “Internet of Everything”

Source: ITU, Mark Lipacis, Morgan Stanley Research - TechSearch
Mobile Products Continue to Get Thinner

Source: ASE.
Wearables: Many Wrist Products

- **Wrist products**
  - Health and fitness tracking bands
  - Watch
- **Contain many sensors to accurately calculate**
  - Heart rate
  - Blood pressure (need higher accuracy) and blood flow
  - Glucose levels
  - Pulse, motion sensing, etc.
- **But, sensors have to function properly!!**
  - Many examples of heart rate or blood pressure sensors that don’t measure accurately
  - Limits product adoption: “Users will stop using the devices and enterprises will not adopt the technology if data is not accurate” according to Morgan Stanley survey

Source: Apple.
Bumping Trends: Moving to Cu Pillar

- **Major OSATs expanding Cu pillar bumping**
  - Amkor
  - ASE
  - SPIL
  - STATS ChipPAC

- **Expanding by China OSATs**
  - JCET/JCAP
  - Nantong Fujitsu
  - Huatian Technology

- **Major foundries with Cu pillar**
  - TSMC
  - GLOBALFOUNDRIES

- **Major IDMs with Cu pillar**
  - Intel
  - Samsung

- **Major transition in fabless**
  - FPGA makers Altera, Xilinx
  - GPU maker nVIDIA
  - ASIC makers AVAGO
  - Wireless: Qualcomm

- **Flip chip on leadframe with Cu pillar**
Drivers for WLP

- **Major applications for WLP**
  - Smartphones (highest volume application)
  - Digital cameras and camcorders
  - Laptops and tablets
  - Medical
  - Automotive
  - Wearable electronics such as watch

- **WLP meets system packaging needs**
  - Small form factor
  - Need for low profile packages
  - Lower cost (less material)

- **Form Factor is key**
  - Low profile
  - Limited space on PCB
It’s Not Just iPhones with Lots of WLPs......

- **Samsung smartphones with WLPs**
  - 6 years ago, no WLPs
  - Galaxy 6S has 13 WLPs on main board

- **Japanese domestic smartphones**
  - Sony Xperia Z4 has 13 WLPs
  - Sharp Aquos Zeta has 13 WLPs

- **China handset makers increasingly using WLPs**
  - Huawei Ascend G620S has 4 WLPs
  - ZTE Goophone has 3 WLPs
  - Even low-end OPPO Joy has one....

- **On average 5 to 7 WLPs per smartphone and the numbers continue to increase......**
Conventional WLP Applications

- Conventional WLPs for many device types (analog, digital, sensor, discrete)
  - Power management IC (PMIC)
  - Audio CODEC
  - RF
  - IPD, ESD protection, filter
  - LED driver
  - Electronic compass
  - Controller
  - MOSFET
  - CMOS image sensors
  - Ambient light sensors
  - EEPROM

- CAGR of almost 9% from 2014 to 2019

- Conventional WLPs trends
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size in HVM Qualcomm PMIC 6.5 mm x 6.5 mm x 0.71 mm, 0.4mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch
  - Fine pitch parts need high-density PCB to route signals

Source: ASE.
FO-WLP: The Rabbit We Are All Chasing
Infineon eWLB Technology

Package 8 mm x 8 mm

Chip: Daisy Chain Test Vehicle
Size: 5 mm x 5 mm
Thickness 450 µm

Package: Size: 8 mm x 8 mm
Balls: 300 µm dia.
196 I/Os
0.5mm pitch

Source: Infineon.
Fan-In and Fan-Out WLP Compared

Conventional WLP (Fan-In)

Fan-Out WLP (package footprint larger than die)

Source: STATS ChipPAC
Drivers for FO-WLP

- Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)
- Thinner than flip chip package (no substrate)
  - Can enable a low-profile PoP solution as large as 15mm x 15mm body
- Support increased I/O density
  - Fine L/S (10/10μm)
  - Roadmaps for <5/5μm L/S, future 2/2μm L/S
- Allows use of WLP with advanced semiconductor technology nodes with die shrinks
  - With increased I/O and smaller die can’t “fan-in” using conventional WLP
  - Smaller diameter balls and ball pitch ≤0.3mm board level reliability issues (Qualcomm studies)
- Split die package or multi-die package/SiP
  - Multiple die in package possible
  - Die fabricated from different technology nodes can be assembled in a single package
  - Can integrate passives
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance

Source: STATS ChipPAC.
Multi-Die/SiP FO-WLP Solution

- 2 Layer-RDL Interconnection
- 2 Active Die + 10 Passives 0201 SMD

Source: NANIUM
Application Processor Packaging Trends

- Thinner package and smaller footprint
  - Today 1.0mm height requirement
  - Future ≤0.8 mm
- 3D IC with TSV provides the ultimate in package height reduction, but continues to be pushed out
- Silicon interposers too expensive for many mobile products
- PoP in high-end smartphones
  - Option 1: Continue with FC on thin substrate
  - Option 2: Embedded AP in bottom laminate substrate
  - Option 3: Fan-out WLP with application processor as bottom package
  - Option 4: Some new format (SWIFT, NTI, etc.)
- FO-WLP AP in bottom PoP
  - Low profile
  - High routing density
  - Handle high power
  - System integration with competitive cost
Potential RF, PMIC, and AP, Migration to FO-WLP

- Modem FCBGA-333 Qualcomm MDM9625M
- RFIC WLP-164 Qualcomm WTR1625L
- RFIC WLP-66 Qualcomm WFR1620
- Audio codec WLP-42 Cirrus 338S1201
- WiFi/BT/FM FLGA-58 Murata 343S0694
- A-CPU PoP-1155 Apple/TSMC APQL-
- PMIC WLP-94 Qualcomm PM8019
- PMIC WLP-28 Qualcomm QFE1100
- M8 Co-pro. WLP-40 NXP LPC18B1UK
- *

Source: TPSS.
Early products included baseband processor (Infineon Wireless Division)
Device types include RF such as Bluetooth, NFC, GPS, PMIC, automotive radar, connectivity modules, future application processors from TSMC and others
Many multi-die products in future
Projecting a CAGR of 87% in unit shipments from 2015 to 2020
Why is FO-WLP A Disruptive Technology?

- **No substrate**
  - Thin-film metallization used for substrate (can go below 5μm L/S)
  - No traditional laminate substrate
  - No underfill
  - Most application processors had been using laminate substrate with flip chip bump interconnect
  - Removes substrate supplier as design partner

- **Infrastructure changes**
  - All packaging can take place at the foundry
  - Assembly can also take place at OSAT but uses a non-traditional OSAT assembly line
  - Requires IC/package co-design

Source: Nanium.
FO-WLP Suppliers Status

- Amkor Technology redeploying FO-WLP with new 300mm line (eWLB) in K4
- ADL Engineering 200mm pilot line in Taiwan
- ASE license for Infineon’s eWLB with 300mm in Taiwan, also offers “chip last” panel version
- Deca Technologies (300mm “panel” format)
- NANIUM (300mm wafer) license for Infineon’s eWLB
- NEPES (300mm line in Korea)
- PowerTech Technology (300mm line future, R&D on panel)
- SPIL (300mm wafer)
- STS Semiconductor and Telecommunications (300mm production line in qualification)
- STATS ChipPAC (300mm wafer) purchased by JCET, license for Infineon’s eWLB
- Samsung (internal production expected)
- TSMC (300mm wafer InFO process)
- All China OSATs will offer versions in future
- YOUR NAME HERE
Alternatives to Reconstituted Wafer FO-WLP

- Amkor’s SWIFT
- ASE’s chip last versions
- Conventional flip chip
- Molded Interconnect Substrate (MIS)
- Embedded die solution/panel processing

Source: Amkor.
SiPs for IoT/IoE Applications

- Expansion of IoT/IoE means an increased number of sensors, but also more connectivity, signal processing, and data storage
- Primary device requirements are low power and low cost
- No single package format
  - Many applications may adopt system-in-package (SiP)
  - Many just SMT modules on FR-4 board, not counted as SiP but as system-in-module (SiM)
- One main reason IoT/IoE is expanding rapidly is the low cost of sensors and multi-die packages and modules

Source: SPIL.
How Do We Define SiP?

- Package containing combination of two or more dissimilar die to create a functional sub-system in a standard format package
  - May include MEMS assembled into a single package
- Typically combined with other components such as
  - Passives
  - Filters
  - Antennas
- Single die with pre-packaged die on a substrate of a package

Source: TPSS.
Reasons for SiP Adoption

- **Miniaturization**
  - Form factor (package height, footprint)
- **Heterogeneous technology integration**
  - RF, analog, power regulator integration
  - Memory integration (buffer/flash) or (high bandwidth)
- **Mixed process technology (90nm, 65nm)**
- **System performance**
  - Noise reduction
  - High speed bus
- **System flexibility, features, and configurability**
- **Total system cost reduction**
  - Package/device cost
  - System cost (board layer count reduction)
  - Development cost
  - Time to market
Drivers for 3D IC

- High future cost of lithography for next generation silicon technology nodes
- Stacking transistors and other silicon developments buys time
- Severe interconnect delay
  - Noted in ITRS roadmap
- Bottleneck for higher bandwidth
- Device latency issues
- Power management, delivery, and distribution needs
Memory Stacks with TSV: New Memory Architectures

- **Tezzaron high-speed memory**
  - Production shipments
  - High-performance applications

- **Micron Hybrid Memory Cube (HMC)**
  - Shipments started in 2015
  - Network systems, GPUs, and other applications

- **Samsung RDIMM with stacked memory for servers**
  - DDR products

- **SK Hynix (HBM)**
  - Stacked die mounted on interposer
  - GPU, etc. applications

Source: Samsung.

Source: SK Hynix.

Source: Micron.
Si Interposer Era: The Beginning

- **FPGA shipments started (HVM 2012)**
  - Xilinx has at least 7 products at 28nm
  - Moving into production on 20nm
  - Expanding from just high-performance FPGAs to mid range FPGAs

- **GPU+stacked memory**
  - AMD Fiji in production (small volumes)
  - nVIDIA product announced

- **ASIC designs moving into production**

- **Applications include network systems and future servers**
  - Applications require high performance
  - Cost/benefit analysis allows adoption
  - Low unit volumes, high dollar value

- **No potential for mobile products**
  - Needs low-cost solution
  - Not currently available

Source: Xilinx.

Source: AMD.
Conclusions

- Future requires co-design between IC designer and package designer
- New designs for next technology nodes in flip chip
- Mobile products require low profile packages
  - Fan-in WLP
  - FO-WLP
  - Growth in FO-WLP will impact FC-CSP
- Demand for lower cost solutions drives adoption of new package designs and formats
- SiP many different packages
  - Many different packages
  - Growing number of companies selecting FO-WLP with reconstituted wafer
- Silicon interposers
  - High-performance applications in volume production
  - Lower cost alternatives under development
Thank you!

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