The Future of HDI Via Structures, Power Delivery, and Thermal Management in Next Generation Printed Circuits

Presented By

Tom Buck
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Today’s advanced electronic systems require a complex blend of many process technologies that must work in concert to provide interconnect solutions ranging from high current DC to millimeter wave radar…

- Laser drilled microvia’s
- Stacked microvia’s
- Blind & Buried vias
- Thermal management techniques
- Heavy copper design
- Embedded busbar technologies
- Precision etching technologies

…The goal of this presentation is to examine emerging PCB technologies and their impact on next generation electronic systems
Today’s Agenda

• Market drivers & what’s driving PCB densities
• Alternate via structures and microvia’s
• NextGen™ Mass terminated microvia
• Thermal management techniques
• High current busbar and heavy copper
• Precision etching technology for RF and Microwave
• Summary and wrap up
Overview

PCB Market Drivers
&
What’s Driving PCB Densities?
Density Trends In Array Packages

Increasing I/O Density

Chip Scale Packaging

Flip Chip Packaging

1.27 mm BGA package
Localized via density 62/cm² (400/in.²)

0.50 mm BGA package
Localized via density 400/cm² (2580/in.²)

0.20 mm Flip Chip
Localized via density 2500/cm² (16,129/in.²)

6.45 x Increase in via density

6.25 x Increase in via density
Increasing Densities in Array Packages

Interposer substrate to transform Silicon geometries to PCB geometries. Most often made with PCB process.

Silicon die encased in molded plastic.

Common BGA Pin pitch:

- 1.27 mm
- 1.0 mm
- 0.8 mm
- 0.75 mm
- 0.65 mm
- 0.5 mm
- 0.4 mm
- 0.25 mm

357 I/O BGA Package

Drilled hole diameter and Pitch are reaching limits and restricting routing.

Through hole PCB
Circuit Density & Mechanical Drilling limitations

Decreasing Channel Density  Technology Shift  Increasing $

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<thead>
<tr>
<th>Drill dia.</th>
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<th>Pad dia.</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 mils</td>
<td>25 mils</td>
<td>10 mils</td>
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<td>5 mils</td>
<td>125 mils</td>
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<td>3.5 mils</td>
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<td>125 mils</td>
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</tbody>
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- Board thickness limited by drill flute length
- Hole barrel reliability with lead free assembly

Standard Production
Mechanical Drilling

- Alignment issues
- Drill wander
- Drill life
- Hole quality

Same process smaller drills!

CNC PCB Drilling Machine
Putting Small Diameter Drills Into Perspective

Human hair

2.5 mil (60 micron) to 3.5 mil (90 micron)

5.9 mil (150 micron)

• Small diameter are very fragile
• High speed spindles are required
• Feed rates are about 50% of standard via diameters
• Drill life of 300 to 600 hits depending on material
• Short flute length limits hole depth
• Drill cost is higher
• Limited availability from offshore PCB production

Carbide drill bit
Array Pattern Escape: Through Hole IPC Class 2

1.27 mm: 3 Track
10 mil drill
20 mil pad
4 mil track

1.0 mm: 2 Track
10 mil drill
20 mil pad
4 mil track

0.8 mm: 1 Track
8 mil drill
18 mil pad
3.5 mil track

0.5 mm: 0 Track
6 mil drill
14 mil pad
No routing

What now?
Laser Drilling Technology

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**Combination ND:YAG CO₂**
Forms holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the CO₂ laser (Approximately 3,500 to 13,000 holes per minute)

**Note:**
1. Hole depth is limited by plating aspect ratio (depth/diameter) Typical aspect ratio on laser drilled holes is 0.5:1 to 0.6:1 max
2. Holes greater than 0.005” are generally considered too large to be placed in component pad

**Typical Via Diameter**

Laser drilled Microvia
Layer 1 to 2

Termination or "Capture Pad"

0.005”
0.006”
0.003”
Array Pattern Routing: Microvia

1.0 mm: 3 Track
5 mil Laser
10 mil pad
4 mil track

0.8 mm: 2 Track
5 mil Laser
10 mil pad
4 mil track

0.5 mm: 1 Track
5 mil Laser
10 mil pad
3 mil track

0.4 mm: 0 Track
5 mil Laser
10 mil pad
No track
Routing is possible with smaller internal pads and sub 3 mil lines reducing yields

What now?
0.4 mm BGA Escape: Fine Line Approach

Advanced Routing (60/60/220)

4 mil microvia/8.66 mil pad
2.36 mil trace/2.36 mil space on plated layers
Routing By Via Row Reduction

Once routing channels are eliminated by current process limitations, each row of the array pattern will require a unique routing layer. As each row is connected it will open routing for the next.

This approach dramatically Increases PCB complexity!
Second Generation Microvia Geometries

Stacked MicroVia (SMV®)
L1-L2, L1-L3 & L1-L4

Stacked MicroVia Landing on a Plated & Non-Plated Layer
Achieving Higher Densities Using Alternate Via Structures
Is Advanced PCB Technology Cost Effective?

Classic Technology Utilization Curves

All technologies have finite limitations! As applications approach their limits, technologies can become ineffective.
Technology Options Extending PCB Densities

Through Hole PCB Technology Limits?

- Mechanical drill size
- Plating aspect ratio
- PTH reliability
- Minimum line width
- Layer count > thickness
- High speed via transitions

Technology Options:

- Via-In-Pad technologies
- Blind via (sequential Lamination)
- Blind and Buried via (sequential Lamination)
- Controlled depth drilling
- Laser Microvia
- Stacked Microvia
- Laser modified controlled depth drill
- NextGen™

Many options will require Enhanced registration & Copper plating capabilities
• Increased channel density on layers below the controlled depth drill
• Standard PTH geometry apply, Depth limited by aspect ratio
• No sequential lamination required
Via hole is first mechanically drilled then with a laser the remaining dielectric is removed clearing a path to the copper layer.

- Increased channel density on layers below the controlled depth drill
- Allows a connection with no stub
- Standard PTH geometry apply, Depth limited by aspect ratio
- No sequential lamination required
Via Structures: Blind Via

- Increased channel density on lower sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- Increased channel density on sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- No Z axis connectivity between adjacent sub-laminations
- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)
- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)
Increasing Density Using Stacked Microvia’s and its Implications
2-4-2 HDI Substrate

First and Second Generation Microvia Structures

- 1:3 μVia
- 1:2 μVia
- 1:3 Stacked plate fill μVia
- 1:2 Plate fill μVia

2 Layer HDI buildup

4 Layer MLB core

1:2 → 2:3 Staircase μVia

First Generation Microvia Structures

Second Generation Microvia Structures
Second Generation Microvia: Solid Copper

Mechanism of via filling

- Bottom-up filling behavior is attributed to the action of organic additives (must be controlled to prescribed limits)
- Suppressor rapidly forms current inhibiting film on Cu surface. Film has little geometric dependence due to high suppressor solution concentration
- Accelerated bottom-up fill behavior is due to a local accumulation of brightener species at the feature base
- As surface area is reduced during deposition, the concentration of brightener species increases, resulting in a non-equilibrium surface concentration. This local concentration of brightener accelerates the plating rate relative to the surface.

Preferred fill Method!

Source: Mechanism of via filling

Planar Microvia

Stacked Microvia

- Brightener
- Carrier
Second Generation Microvia Geometries:

Example 1: Two layer stacked microvia (+2) terminating on a copper foil shown with a copper plat fill on the layer 1 to layer 2 via for via-in-pad application. H1 and H2 represent the dielectric thickness between layers and standard design rules apply.

Example 2: Two layer stacked microvia (+2) terminating on a plated layer. This example illustrates how the internal solid copper via’s become the building block for the via’s on top until you get to the layer 1 to 2 via. The final 1 to 2 via has the option to be filled with copper (recommended for via-in-pad) or they can be left as a standard via with a divot if used as an interstitial via. H1 and H2 represent the dielectric thickness between the layers where standard microvia rules apply.
Chip Scale BGA Escape Using Stacked Microvia

Section A-A: 4 layer stacked microvia structure*

* Only top 5 layers of the board are shown
Viasystems is constantly working to enable new technologies to meet the needs of high-technology customer demands with small, feature rich products (ex. mobile phones, PDA, cameras, and other such products).

- Viasystems continues to drive technology enhancements in the SMV™ arena:
  - Requires one to two lamination cycle (based on design constraint), reducing fabrication time
  - Eliminates plating cycle of inner layers
  - Improves inner layer characteristics, signal integrity and electrical characteristics
  - Reduces demand on plating and lamination, improving facility capacity utilization
  - Allows for thinner finished product
  - Initial customer builds have been encouraging with significant early interest
  - This is a Viasystems patented technology
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Step 1. Single sided core

Step 2. Single sided etched core

Step 3. Adhesive and single sided etched core

Step 4. Laser drilled micro vias

Step 5. Filled micro vias

Step 6. After single lamination

- Laminate
- Protective film
- Metallic paste filler
- Copper foil
- Film adhesive
NextGen-SMV™ vs. Conventional SMV™

**Single Lamination Parallel Process (SLPP™)**

**NextGen**

- Single Lamination
- Stacked Via

**Conventional**

- Sequential Lamination
- Stacked Via

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**Material Issue**
- Triacid Chemclean
- LDI Resist Coat
- LDI Expose
- Develop, Etch, Strip
- Alternate Oxide
- HRL/CSL Adhesive
- PEP
- Laser Via Generation
- Via Fill
- Layup and Laminate

**LDI Resist Coat**
- Laser LDI Tooling
- Pumice Scrub
- LDI Resin Coat
- LDI Expose
- Develop, Etch, Strip

**Alternate Oxide**

**Soldermask, Final Finish, Legend, Fab**

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**Photoprint Dots**
- Develop Dots
- Plate Microfill
- Resist Strip
- Planarize
- B/S Electroless
- LDI Resist Coat

**Etch**
- Pattern Plate Copper
- Solder Plate
- Resist Strip
- Solder Strip

**Etch**
- Pattern Plate Copper
- Solder Plate
- Resist Strip
- Solder Strip

**Repeat for**
- Sub 1 to 10
- Sub 3 to 9
- Sub 4 to 7
- Sub 4 to 7
- Sub 3 to 9
- Sub 1 to 10
HDI-Link™ - Sub-to-Core Attach

Potential solution to add multiple HDI layers to a buried via, ex. 3+N+3

Patent Pending
Sub-Link™ - Sub-to-Sub Attach (Sub A, B, C, …)
Solution for High Aspect Ratio PCB, > 33:1 AR

Multiple Standard multi layer subs after Lamination Process

Patent Pending
Overview

Advanced Thermal Management Techniques
Thermal Conduction In PCB’s

Heat Flow

Thermal resistance at each level of an electronic system will impact conduction…

…Heat generated must go somewhere!

Relative surface area
Factors Increasing Thermal Density

- Dramatic increase in Semiconductor power
- Rapid reduction in component size

Power dissipation 3 watts
Power density 1.08 watts/cm

Density increase

Power dissipation 3 watts
Power density 3.7 watts/cm
Thermal Conductivity

Thermal conductivities of common PCB materials

- Copper: 0.3 W/m · K
- Silver: 1.0 W/m · K
- Gold: 0.64 W/m · K
- Nickel: 0.6 W/m · K
- Aluminum: 0.4 W/m · K
- Solder: 0.3 W/m · K
- Stablcor: 10 W/m · K
- FR-4: 1.0 W/m · K
- Ceramic: 0.3 W/m · K
- CB-100: 1.0 W/m · K
- TC350: 0.6 W/m · K
- RO4350: 0.3 W/m · K

ST10: 10 W/m · K
PCB’s are composed of resin, glass and a random distribution of copper that is parallel to the PCB surface. An approximate value for parallel and perpendicular conductivity are:

\[ K_{II} = 27.5 \text{ W/mK} \]
\[ K_{\perp} = 0.41 \text{ W/mK} \]

Approximations are based on FR4 based laminate and will vary based on actual board construction and specific distribution of copper! But they are a good starting point.
PCB Thermal Resistance: Parallel

Example:
PCB 15.25 mm x 22.9 mm
(6” x 9”)

\[ R_{\parallel} = \frac{L}{K \times A} = \frac{11.45 \times 10^{-3}}{27.5 \times 1.6 \times 10^{-3} \times 15.25 \times 10^{-3}} = 17.06 \text{ K/W} \]

The example does not take into account the thermal resistance from the IC and perpendicular resistance in the PCB.

Note: This example assumes Z axis conductivity
Component (Heat Source)
1.0 cm (0.394")

PCB R⊥ approximately
0.41 W/mK

PCB Substrate 1.6 mm (0.063")

Example:
PCB 15.25 mm x 22.9 mm
(6” x 9”)

Note: This example only accounts for
the conductivity of the substrate
in the Z axis

$$R_\perp = \frac{L}{K \times A} = \frac{1.6E^{-3}}{0.41 \times (10E^{-3})^2} = 39 \text{ K/W}$$

Relatively large thermal resistance in the Z axis since copper
layers are separated by high resistance laminate
Common dielectric materials have relatively low thermal conductivities where as electrical conductors have relatively high conductivities…

![Diagram showing heat flow between dielectric materials and electrical conductors.]

Dielectric materials: 0.3 to 1.0 W/mK
Electrical conductors: 25 to 400 W/mK

…Increased thermal conductivity is achieved with conductors
Thermal Via Applications

Thermal pad for conducting head from the component to internal planes or external heat sink on the back of the board

Plated through hole provide a thermal shunt resistance bypassing the dielectric layer

Issues: Through holes will wick solder away from the component connection and deposit on the back side of the board!
Thermal Resistance: Parallel Thermal Via’s

Thermal resistance $K/W$

Parallel Thermal Via’s Through 0.062" (1.6mm) FR4 Substrate

Drill diameter
- 0.008" (0.2mm)
- 0.012" (0.3mm)
- 0.016" (0.41mm)
- Copper Plating (0.020" (0.51mm))

Note: Thermal via’s placed in a 1.0 cm (0.0394) square
Common thermal via constructions:

- **Standard**
  - Diameter: 0.001”

- **Conductive Filled**
  - Diameter: 0.001”, Conductive filler thickness: 0.002”

- **Thicker Copper**
  - Diameter: 0.002”

Copper = 380 W / m K
Conductive filler = 3.5 to 6.7 W / m K
Thermal Resistance vs Via Technologies

Thermal resistance K/W

Drill diameter
- 0.001" (0.025 mm) copper plating
- 0.001" (0.025 mm) copper plating conductive filler 6.7 W/mK
- 0.002" (0.05 mm) copper plating

All plated through holes 0.012" (0.3 mm) dia.

Thermal via length in mm

0 0.5 1 1.5 2 2.5 3

100 200 300 400 500 600
Solid copper Thermal Via’s

Solid Copper Via

- Process to provide solid copper fill at accelerated plating rates
- 10:1 aspect ratios are currently achievable
- Applications include:
  - Low resistance via’s allowing high current or reduced diameter
  - Thermal via’s with high conductivity
  - Potential replacement for wrap plating
Thermal Resistance Parallel Via’s

Thermal resistance K/W

Parallel Thermal Via’s Through 0.062” (1.6mm) FR4 Substrate

Drill diameter
- 0.010” (0.25mm) Solid
- 0.008” (0.2mm) Solid
- 0.006” (0.15mm) Solid
- 0.010” (0.25 mm)
- 0.008” (0.2mm)
- 0.006” (0.15mm)

Both have the same relative thermal conductivity

Note: Thermal via’s placed in a 1.0 cm (0.0394) square
Bonded Heat Sinks

• Thermal via-farms

• Heat-transfer underneath component through the PCB to spread heat to inner layer copper-planes and / or opposite side of PCB where external heat sink or housing.
Thermal Management

Pre cut pressure sensitive adhesive

Machined heat sink

Bare Board

Composite assembly

Aluminum and Copper Heat sinks post-attached to finished PCBs using Pressure Sensitive Adhesive Tapes.
Embedded Copper Coins

• Press Fit Coin (PFC) (Inlay)
  • Cu coins are mechanically “Press Fit” or “Inlayed” into the PCB during manufacture.
  • Good for applications requiring improved thermal heat transfer over traditional via-farms.
  • Coin shape can be designed for almost any application
    • Automotive – Round coins (hot spot cooling), drilled openings offer tighter size control
    • PA devices – Rectangle coins offer customized coin options while still maintaining good coin retention
Thermal Management

Thermal Conductivity: via-farm vs solid copper embedded coins

Thermal resistance through the board = 1.3 K/W

Thermal resistance through the board = 0.05 K/W
• Embedded Copper

- Similar in configuration to press fit, these copper coins are inserted during the lamination process
- The coin is retained in the coin opening by the resin of the PCB material and thus becomes an integral part of the PCB
- Can be drilled and plated as part of the PCB
- Similar applications as press fit with good thermal heat transfer
• **E-Coin** (Viasystems Patented)

  - Cu flanged coins are inserted during the lamination process becoming an integral part of the PCB
  
  - Excellent coin to PCB grounding capabilities
  
  - Applications where both electrical (grounding) and thermal requirements are needed.
  
  - Excellent planarity of coin to PCB surface
Surface Attached Copper Coin

- Sweat Solder
  - Post coin attach of pallet and coin heat sinks utilizing solder attach as the bond system
- Post coin/pallet attach utilizing thermally/electrically conductive adhesive
  - Copper/Au plated coins attached after PCB build completion
Integrated High Current Applications
&
Thermal Planes
External conductors. Copper-plate & Etch technology

- If solder mask coverage is required (min 5um), the max. total copper thickness is 210um (6Oz)
- Special solder mask ink and process (E-Spray) is recommended to reduce risk on solder mask-cracking.
- Due to copper thickness and CTE mismatch solder mask cracking during Thermal Cycling can not be avoided.
- PCB design (copper and solder mask) have huge impact on cracking of solder mask.
- For critical applications we recommend to use extreme heavy copper only on inner-layers.

8.3 mils (210um) final copper thickness on external layers
Heavy Copper Outer-layers

Design recommendations

- External conductors. Copper-plate & Etch technology
  - Copper Layout has influence on cracks in solder mask.
  - Sharp corner in copper create stress-points increasing risk on solder mask cracks.

Good; rounded corners in copper pattern

Not Good; sharp corners in copper pattern
Solder Mask Design Recommendations

- Solder mask design;
  - Solder mask design has influence on cracking.
  - Sharp corner in solder mask-design create stress-points increasing risk on solder mask cracks.
Solder mask & Gap Filler for 12 Oz Outer Layer

Challenge: Solder Mask coverage & thickness at trace corner

Resolution: Gap Filler filling by stencil screen printing

Etched 12 oz Outer layer

Polymer filling Of the etched gap

Planar surface after solder mask
### Copper Feature Capabilities - Outer-layers

#### Etch Capability vs Base Copper Weight

<table>
<thead>
<tr>
<th>Etch Capability</th>
<th>Oz (mil)</th>
<th>1/8</th>
<th>1/4</th>
<th>1/3</th>
<th>1/2</th>
<th>1</th>
<th>2</th>
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<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>(um)</td>
<td></td>
<td>5</td>
<td>9</td>
<td>12</td>
<td>18</td>
<td>35</td>
<td>70</td>
<td>105</td>
<td>140</td>
<td>175</td>
<td>210</td>
<td>245</td>
<td>280</td>
<td>315</td>
<td>350</td>
<td>385</td>
<td>420</td>
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<td>3 / 4</td>
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<td>4 / 5</td>
<td>100/125</td>
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<td>7 / 7</td>
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<tr>
<td>8 / 8</td>
<td>200/200</td>
<td></td>
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<td>9 / 9</td>
<td>225/225</td>
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<td>10/10</td>
<td>250/250</td>
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<tr>
<td>12/12</td>
<td>300/300</td>
<td></td>
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<td>14/14</td>
<td>350/350</td>
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<td>16/16</td>
<td>400/400</td>
<td></td>
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<tr>
<td>20/20</td>
<td>500/500</td>
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<td>24/24</td>
<td>600/600</td>
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<td>26/26</td>
<td>650/650</td>
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<td>28/28</td>
<td>700/700</td>
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- **Production (volume)**
- **Leading Edge (limited)**
- **Development**
Heavy Copper Inner-layers

Internal conductors (print-and-etch)

Example:
- 6L product application
- Two cores with two 10oz/10oz copper layers based on print and etch process
- SEM pictures taken after solder shock
- High reliability demonstrated

Example:
- 4L product application
- One core with two 410um (12 Oz) copper layers based on print and etch process
- SEM pictures taken after solder shock
- High reliability demonstrated

To avoid reliability-issues with extreme heavy copper on outer-layers we recommend to move heavy copper to inner layers.
Copper Feature capabilities Inner-layers

<table>
<thead>
<tr>
<th>Etch Capability</th>
<th>Base Copper Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>(mil)</td>
<td>Oz 1/4 1/3 1/2 1 2 3 4 5 6 7 8 9 10 11 12</td>
</tr>
<tr>
<td>(um)</td>
<td>9 12 18 35 70 105 140 175 210 245 280 315 350 385 420</td>
</tr>
</tbody>
</table>

- **Width / Space**
- **Base Copper Weight**
- **Production (volume)**
- **Leading Edge (limited)**
- **Development**
Incorporating Heavy Copper Foil

Signal via through Cu core

Thermal via

Blind via

Heavy copper foil used as a thermal path

Surface edge rails
Approximating Thermal Resistance

When there is a temperature difference, heat will flow.

Heat flow in

Hot interface

X = Y = Square

Cold interface

Heat flow out
Copper Foil Thermal Resistance

Thermal resistance per square K/W

Copper foil thickness in microns

ED Copper foil
- 1/2 oz Foil 0.0006" (15 micron)
- 1.0 oz Foil 0.0012" (30 micron)
- 2.0 oz Foil 0.0024" (61 micron)
- 3.0 oz Foil 0.004" (101 micron)
- 4.0 oz Foil 0.0054" (137 micron)
High Current Applications
&
Embedded Busbar’s
Traditionally, high current busbars have been placed externally on PCB’s making it difficult for higher density integrated power designs.
Embedded Busbar Technology

• Increasing current as well as thermal dissipation are driving the need for copper thicker

• When copper thickness exceeds practical etching technologies embedded bus-bars become practical

• Embedded busbars take advantage of the fact that they can pre-machined with precision prior to board fabrication

• Once the board is fabricated the bus-bar becomes an integral part of the finished PCB
Embedded Busbar Technology

Copper stock → Precision machining

Pre-machined Busbar → Finished PCB
Use a 5L stack-up (a few layers without copper). 2 cores & 2 layers of copper foil are used, use prepreg to fix the Busbar and ensure no resin void around the Busbar. (refer to the stack-up bellow).
PCB Design; L1 Solder Mask and Cavities.

3 busbar leads which extend the PCB must be reduced in thickness by controlled depth routing

L1 Pattern (red)

Soldermask clearances (yellow)

4 cavities to be created by depth controlled routing to expose busbar (blue)

Cavities will (during assembling) be filled with solder and soldered to Mosfet body for conducting electrical current and heat.
Lamination process

Pre routed core

Copper Busbar

prepreg

Composite substrate with embedded busbars
Busbar Cross-Section

- There is no gap and void between busbar and laminate.
- Resin completely filled the gap.
Finished Circuit

Top side view

Bottom side view
C²eT
Controlled Copper Etch Technology
Precision Features For RF and Microwave Applications
• RF and microwave circuits generally require printed components such as antenna, filters, couplers, resonators and precision taps
• As frequencies increase printed component size decreases with a demand for improved conductor resolution i.e. precise trace and space
• Current designs are demanding finished trace and space tolerance to be +/- 0.0005” to 0.0007” (predicated on customers demand for performance)
• Pattern plating on surface layers reduced conductor resolution
• Via-In-Pad required in many designs introduces wrap plating, increasing the background copper that must be etched, further reducing resolution
• Producing Foil Only etched features eliminates the plating and wrap plating in feature regions improving resolution
Pattern plating process for via plating and non-critical circuit formation

Filter image etched into Outer layer foil, no plating

Mask overlap region; typically 6 mils
Sample stack-up of RF & Microwave job

Layer 1
Laminate Core

Layer 2
Prepreg
RF Signal Layer

Layer 3
Laminate Core
Mixed Signal Layer

Layer 4
Mixed Signal Layer

Mechanical drill standard pattern plating

Foil only region

Laser drill standard pattern plating

Rogers 6002 0.010”
1/2 oz + Plt
1/2 oz
370 HR 2X 106

370HR 0.008”
1/2 oz
1/2 oz + Plt
Example of PCB Outer Layer

RF Outer Layer With Printed Filters

- Foil region consists of only foil and Cu flash plate
- Pattern plate region, standard copper thickness
- Photo tools are required for:
  - Foil only print and etch
  - Pattern plate tools with foil only isolation
  - Foil only photo tool to protect Foil Only region in final etch
Foil Only regions defining printed RF components

The defined regions will be Foil Only for precise etching. Copper consists of only foil and Cu flash plate in the case of Teflon outer layer dielectric materials such as the Rogers 6002 used in this example.
Pattern Plate Artwork

Critical interface between the Foil Only region and the raised copper pattern plate surface

Illustration of Foil Only and pattern plate definition

Foil Only regions are masked with LDI photo resist during the pattern plate process

Pattern plate image
Foil Only Features On Surface Plated Layers

Standard copper pattern plate

Trace cross-section A-A

Plated region
Transition region
Foil region

Transition region

Foil only region

A

A
First Pass Line Width Tolerance: Foil Region

- Line widths were evaluated on non-compensated etched traces
- Average values were obtained yielding a tolerance based on the difference from the average values. First pass results better than +/- 0.0005”

<table>
<thead>
<tr>
<th>Board #</th>
<th>A-1 (line)</th>
<th>A-2(space)</th>
<th>A-3(line)</th>
<th>B-1(line)</th>
<th>B-2(space)</th>
<th>B-3(line)</th>
<th>C-1(line)</th>
<th>C-2(space)</th>
<th>C-3(line)</th>
<th>D-1(line)</th>
<th>D-2(space)</th>
<th>D-3(line)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>9.00</td>
<td>13.00</td>
<td>9.00</td>
<td>9.00</td>
<td>13.00</td>
<td>9.00</td>
<td>7.00</td>
<td>5.00</td>
<td>7.00</td>
<td>7.00</td>
<td>7.00</td>
<td>5.00</td>
</tr>
<tr>
<td>1</td>
<td>8.43</td>
<td>13.49</td>
<td>8.57</td>
<td>8.5</td>
<td>13.42</td>
<td>8.44</td>
<td>6.6</td>
<td>5.41</td>
<td>6.53</td>
<td>6.61</td>
<td>5.27</td>
<td>6.45</td>
</tr>
<tr>
<td>2</td>
<td>8.5</td>
<td>13.42</td>
<td>8.56</td>
<td>8.71</td>
<td>13.43</td>
<td>8.64</td>
<td>6.74</td>
<td>5.27</td>
<td>6.61</td>
<td>6.75</td>
<td>5.34</td>
<td>6.47</td>
</tr>
<tr>
<td>3</td>
<td>8.64</td>
<td>13.35</td>
<td>8.71</td>
<td>8.64</td>
<td>13.42</td>
<td>8.57</td>
<td>6.84</td>
<td>5.2</td>
<td>6.85</td>
<td>6.68</td>
<td>5.41</td>
<td>6.68</td>
</tr>
<tr>
<td>4</td>
<td>8.57</td>
<td>13.49</td>
<td>8.5</td>
<td>8.57</td>
<td>13.28</td>
<td>8.57</td>
<td>6.53</td>
<td>5.34</td>
<td>6.61</td>
<td>6.61</td>
<td>5.48</td>
<td>6.53</td>
</tr>
<tr>
<td>5</td>
<td>8.57</td>
<td>13.35</td>
<td>8.71</td>
<td>8.64</td>
<td>13.21</td>
<td>8.71</td>
<td>6.54</td>
<td>5.27</td>
<td>6.67</td>
<td>6.47</td>
<td>5.48</td>
<td>6.47</td>
</tr>
<tr>
<td>6</td>
<td>8.71</td>
<td>13.28</td>
<td>8.64</td>
<td>8.64</td>
<td>13.21</td>
<td>8.73</td>
<td>6.81</td>
<td>5.13</td>
<td>6.82</td>
<td>6.6</td>
<td>5.27</td>
<td>6.68</td>
</tr>
<tr>
<td>7</td>
<td>8.57</td>
<td>13.42</td>
<td>8.64</td>
<td>8.57</td>
<td>13.35</td>
<td>8.64</td>
<td>6.6</td>
<td>5.27</td>
<td>6.6</td>
<td>6.61</td>
<td>5.41</td>
<td>6.53</td>
</tr>
<tr>
<td>8</td>
<td>8.5</td>
<td>13.42</td>
<td>8.5</td>
<td>8.5</td>
<td>13.56</td>
<td>8.57</td>
<td>6.46</td>
<td>5.55</td>
<td>6.53</td>
<td>6.46</td>
<td>5.41</td>
<td>6.47</td>
</tr>
<tr>
<td>9</td>
<td>8.78</td>
<td>13.28</td>
<td>8.65</td>
<td>8.65</td>
<td>13.42</td>
<td>8.64</td>
<td>6.96</td>
<td>5.06</td>
<td>6.89</td>
<td>6.61</td>
<td>5.27</td>
<td>6.67</td>
</tr>
<tr>
<td>10</td>
<td>8.71</td>
<td>13.29</td>
<td>8.62</td>
<td>8.5</td>
<td>13.45</td>
<td>8.57</td>
<td>6.48</td>
<td>5.55</td>
<td>6.6</td>
<td>6.54</td>
<td>5.41</td>
<td>6.53</td>
</tr>
<tr>
<td>Diff from Avg.</td>
<td>-0.40</td>
<td>0.38</td>
<td>-0.39</td>
<td>-0.41</td>
<td>0.38</td>
<td>-0.39</td>
<td>-0.34</td>
<td>0.31</td>
<td>-0.33</td>
<td>-0.41</td>
<td>0.37</td>
<td>-0.45</td>
</tr>
</tbody>
</table>
Finished Hybrid PCB With Foil Only Features
Today’s advanced electronic systems require a complex blend of many process technologies that must work in concert to provide interconnect solutions. Good engineering and careful planning lead to quality results…

• Start designs by defining the technology limiting packages
• Look for a power delivery solution first
• Define the minimum technology set for the PCB design
• Review the design interactions with the technologies selected
• Make sure the technology level is compatible with your PCB supply chain
• Rethink design strategies before “bending” the rules

…Sometimes a little more time spent on a design can dramatically reduce cost
Thank You!

tom.buck@viasystems.com