Design for ESD Prevention & ESD Failure Analysis Techniques

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Cheryl’s Background

- 22 years in Electronics
  - IBM, Cypress Semiconductor, National Instruments
  - SRAM and PLD Fab (silicon level) Printed Circuit Board Fabrication, Assembly, Test, Failure Analysis, Reliability Testing and Management
  - ISO audit trained, ASQ CRE, Senior ASQ & IEEE Member, SMTA, iMAPS

- Random facts:
  - Rambling Wreck from Georgia Tech
  - 14 year old son David, Husband Mike, Chocolate Lab Buddy
  - Marathoner & Ultra Runner
    - Ran Boston 2009 in 3:15
    - Ran 100 miles in 24:52 on 2/4-2/5, 2012
  - Triathlete – Sprint, Olympic, and Half. Ironman finisher in CDA, Idaho in June ‘10
ESD Protection is necessary at the IC, component package and system level

- Different approaches are needed to achieve reliable protection

Designing for ESD impacts both the product design and the manufacturing process controls

What technologies are available to assure a reliable ESD protected product?

- At the IC level
- At the component package level
- At the system level
Good General Design Practices for ESD Prevention

- Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  - Identify all ESD Sensitive Parts on drawings
  - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
- Consider the entire System (Design) as ESD Sensitive
- Use ESD Protection on all susceptible parts (not just System I/Os)
  - Box or System I/O
    - ESD Rating < Class 2 IEC 1000-4-2 (4000V) MANDATORY
  - Internal Components (not exposed to outside connectors)
    - ANSI/ESDA/JEDEC JS-001-2011, Human Body Model (HBM) - Component Level
      - ESD Rating <= Class 1 MANDATORY
      - ESD Rating < Class 2 WHEREVER POSSIBLE
High Speed, RF and GaAs parts will be particularly sensitive to ESD

GaAs Parts are typically rated as Class 0 (<250V) or Class 1A (<500V) – ONLY THE BEST PROTECTION DESIGN AND HANDLING PROCEDURES WILL PREVENT DAMAGE TO THESE PARTS!

Reference: ANSI/ESDA/JEDEC JS-001-2011: Human Body Model (HBM) - Component Level

Place ESD sensitive components and traces to avoid locations where the board may be handled

Consider ESD as well as RF shielding

Where possible install protective devices before ESD sensitive parts

Avoid Coupled ESD events – Do not route traces to ESD sensitive parts near lines connected to the outside world
ESD Design Practices (cont.)

- Perform Circuit analysis to insure effectiveness of ESD protection (Class 2 ANSI/ESDA/JEDEC JS-001-2011 for internal, IEC 1000-4-2 level 2 for I/O)
- Test Boards and Systems for Internal and I/O ESD tolerance
- ESD Protection devices must be connected to a good ground to accommodate up to 30A ESD spikes.
  - If upset of operating circuits is to be avoided, a separate Earth ground should be used
ESD Sensitive Parts (Pin Sensitivity)

- Any pin of a discrete ESD sensitive part (FET, Transistor, etc) may need protection (if not connected to a supply)
  - Input pins
    - Can be sensitive since they have little or no built-in ESD protection
    - Especially on high speed devices like GaAs ICs or discretes,
  - Pins other than inputs (on an ESD sensitive part)
    - Can also be sensitive because an ESD pulse can affect internal voltage levels
    - Any improperly terminated or unprotected pin can be a conduit for ESD
  - Supply pins
    - Provide reference bias connections
    - Should not need additional protection (as long as they are connected to the power supply)
  - Outputs of logical or functional parts designed with active (usually buffered) output stages
    - May have clamping diode protection to the supplies and may not need additional protection – check the part ESD rating
Evaluate Potential ESD

- If ESD sensitive parts are used in design, the circuitry connected to device pins should be evaluated
  - Insure that it provides “attenuation” to prevent voltage in excess of the parts ESD rating from developing in case the pin or connected traces are contacted during board handling or system assembly.

- Often the recommended circuit components for operation of the part will provide adequate ESD protection.
  - This should be verified by analysis or simulation and extra protection added as required to limit the voltage seen at the part.

- Assumptions for analysis/simulation
  - 2000V, 1.5K, 100pf for Internal circuits
  - 4000V, 330 Ohms, 150pf for I/Os
Design for ESD Prevention: ESD IC Device Specifications

- What should you be concerned about?
  - Completely different specification methods for ESD protection of components are commonly used
  - Designers may need to gather comparable data points from differing graphs and tables.
  - Some differentiators to look for and investigate further are outlined below

- IEC Rating: Verify that the ESD protection device is guaranteed to meet or exceed specifications in IEC 61000-4-2.

- Contact versus Air Discharge: Verify that identical specifications are being compared. Some devices are documented with high air discharge ratings, which can be incorrectly compared with the normally lower contact discharge ratings. Contact ratings are fairly repeatable, whereas air ratings vary.

<table>
<thead>
<tr>
<th>IEC 1000-4-2 COMPLIANCE LEVEL</th>
<th>MAX TEST VOLTAGE, CONTACT DISCHARGE (kV)</th>
<th>MAX TEST VOLTAGE, AIR DISCHARGE (kV)</th>
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</table>

- Clamp Voltage: Choose a device with a maximum clamp voltage at a given peak current well below the level that the protected devices can tolerate. The lower, the better.

- Pulse Current: Beware of misleading approximations of peak power capacity. It can usually be improved by specifying a shorter peak duration.
ESD IC Device Specifications

- **Response Time:** Faster-acting devices reduce the width of the pulse transferred, and these devices can help attenuate the peak clamp voltage.

- **Parasitic Capacitance:** Added capacitance degrades I/O signal rise and fall times. On lower-speed signals, this stray capacitance can be lumped into or can displace the need for EMI capacitors.

- **Parasitic Inductance:** Higher impedance in the clamp path (to VDD or ground) can increase the effective system clamp voltage.

- **Multistrike Capability:** Verify that the protection designed-in can survive the expected life of the system. Resultant field failures are difficult to diagnose and can manifest themselves in unexpected functional errors, or even data loss.

- **Integration and Matching:** High-speed differential signals, such as in IEEE 1394, benefit from matched loading on the positive and negative lines of each pair. ESD protection products with multiple devices per package (such as thin-film silicon) can have intrachip device-to-device parasitic impedance matching of less than 0.1%. Unitary packages, however, may vary as much as 30% interchip matching. Printed-circuit-board (PCB) signal routing restrictions may also indicate a need for tight multidevice integration.
Design for ESD Prevention & IC Design Rule Checking

- Many ESD design rules
- Two common types of design rule verification/compliance
  - Design Rule Checking (DRC): standard DRC tools with ESD marking layers
    - Example: Mentor Graphics Calibre PERC
      - Rule 1: Primary Protection for I/O Pad
        - For each net in design, IF net is connected to IO Pad THEN check for up HBM diode and down HBM diode IF diode(s) missing THEN ESD Error
      - Rule 2: Secondary Protection for I/O Pad
        - For each net in design, IF net is connected to input buffer and IO Pad THEN check for CDM up diode and CDM down diode check if CDM resistor exists and is correct value IF diode(s) missing or resistor incorrect THEN ESD Error
    - Net-oriented: in-house tools for circuit analysis.
ESD Protective Device Options

- **Passive Networks**
  - Capacitors – Simple, Low cost
  - Band-pass filters – Somewhat more complex, good ESD protection

- **For lower speed devices**
  - Schottky Diodes – Simple, but capacitance loads HF circuits
  - Diode Clamping Arrays – Good for LF circuits and outputs

- **For higher speed devices (requiring low capacitance)**
  - Low capacity protection diodes (<1 pf) – Robust, Good HF compromise
  - Polymer ESD (PESD) Protection devices (<0.25 pf)
    - Excellent HF characteristics, small size 0402, 0603
    - PESDs have limited Pulse life, good parts withstand 100 to 1000 strikes
    - Operating voltage typically 5V, available to 12V, Trigger Voltage 100, 150V
Simple Capacitive Protection

- Use to provide ESD protection on bypassed pins for ESD sensitive devices, or at Supply input connections
  - Make sure capacitance (C2) is significantly larger than the Human Body Model (>> 150pf) to minimize developed voltage (approx 28 times or 4000pf for protection of a Device with an ESD sensitivity of 150V)
  - May add a Resistor to bleed off charge (from C2)
  - Use 200V rated Cap (for C2)
Filters

- Band-pass filters can be used for higher frequency applications and can be effective for RF system inputs
- Very Robust circuit with good protection

Band-pass Filter 850-2GHz, 50 Ohm Impedance
C1,C2,C3 rated at 100V
Protection with Clamping Diodes

Protection Diode Array (CM1213-01)

ESD at output is clamped at approximately 14V with 4000V ESD hit through 330 Ohm resistance
PESD (Polymer ESD) plus Inductor

- The Inductor shunts lower frequency energy to ground, removing stress from the PESD.
- Provides better protection than the PESD alone and extends life of the PESD.
- The PESD can be used alone for wider bandwidth operation.

IEC HBM

PESD, Trigger Voltage = 150V

D2
Isat (IS): 1E-10
Egap (EG): 1.11
Emis (N): 1.2
Ipulse (XTI): 3.0
Resist (RS): 1.0
Vbreak (BV): 150
Cjunc (CJO): 0.2pF

R1 330

Vs1 DC: Volts undefined
AC: Volts 1.0 AC: Phase
Tran: Pulse 0 to 4000
Distort: Sine undefined

DfR Solutions
Summary of ESD Design Guidelines

- Design ESD Protection for External (System) I/Os to IEC HBM Class 2 (4000V, 150pf, 330 Ohm) Including:
  - RF or signal inputs
  - Control and System I/Os that DO NOT have built in protection to the required limit
- Design ESD Protection for Internal ESD sensitive parts to meet ANSI/ESD S20.20
- Know the ESD rating of every part used
- Select parts (where possible) to meet ANSI/ESDA/JEDEC JS-001-2011-:Human Body Model (HBM) - Component Level 2
  - Parts rated less than Class 2 should have additional protection circuitry added to protect the board during handling
ESD Design Guidelines (cont.)

- For External (System) Inputs use Robust protection:
  - Band pass filter
  - PESD plus Inductor (for Severe condition use PESD + Filter)
- For Internal ESD Sensitive pins use:
  - Single bypass Cap (where possible)
  - Filter if needed
  - PESD or PESD plus Inductor
- Any Pin of an ESD sensitive part may be at Risk If It is NOT:
  - Connected to a supply plane
  - Adequately decoupled to GND (~4000pf @200V)
  - Protected by a “filter” network (simulate for an ESD hit)
- External (System) Output or I/O
  - Use low capacitance Clamping diodes (1pf)
  - PESD if required for speed (.25pf)
ESD Failure Mechanisms, Analysis and Tools
General Words of Wisdom on FA

Before spending time and money on Failure Analysis, consider the following:

- Consider FA “order” carefully. Some actions you take will limit or eliminate the ability to perform follow on tests.
- Understand the limitations and output of the tests you select.
- Use partner labs who can help you select and interpret tests for capabilities you don’t have. Be careful of requesting a specific test. Describe the problem and define the data and output you need first.
- Pursue multiple courses of action. There is rarely one test or one root cause that will solve your problem.
- Don’t put other activities on hold while waiting for FA results. Understand how long it will take to get results.
- Consider how you will use the data. How will it help you?
  - Information?
  - Change course, process, supplier?
  - Don’t pursue FA data if it won’t help you or you have no control over the path it might take you down. Some FA is just not worth doing.
Failure Analysis Techniques

- Returned parts failure analysis always starts with Non-Destructive Evaluation (NDE)
- Designed to obtain maximum information with minimal risk of damaging or destroying physical evidence
- Emphasize the use of simple tools first
- (Generally) non-destructive techniques:
  - Visual Inspection
  - Electrical Characterization
  - Time Domain Reflectometry
  - Acoustic Microscopy
  - X-ray Microscopy
  - Thermal Imaging (Infra-red camera)
  - SQUID Microscopy
Failure Analysis Techniques

- Destructive evaluation techniques
  - Decapsulation
  - Plasma etching
  - Cross-sectioning
  - Thermal imaging (liquid crystal; SQUID and IR also good after decap)
  - Surface/depth profiling techniques: SIMS-Secondary Ion Mass Spectroscopy, Auger
  - OBIC/EBIC
  - FIB - Focused Ion Beam
Electrical Characterization: Components

- Most critical step in the failure analysis process
  - Can the reported failure mode be replicated?
  - Persistent or intermittent?
  - Intermittent failures often incorrectly diagnosed as no trouble found (NTF)
  - Least utilized to its fullest extent
  - Equipment often shared with production and R&D

- Parametric characterization
  - Comparison of performance to datasheet specifications

- Curve tracer
  - Applies alternating voltage; provides plot of voltage vs. current response
  - Valuable in characterizing diode, transistor, and resistance behavior

- Time domain reflectometry (TDR)
  - Release and return of electrical signal along a given path
  - Measurement of phase shift of return signal indicates potential location of electrical open

- Other characterization equipment
  - Inductance/capacitance/resistance (LCR) meter
  - High resistance meter (leakage current < nA)
  - Low resistance meter (four wire; < milliohms)
Examples of Lab Testing

- Electrostatic discharge test – Human body model
- Test method was MIL-STD-883, method 3015.8

Figure 1. Prestress test positive pulse waveform.

Figure 2. Post stress test positive pulse waveform.
Results

Electrical

Curve tracing was done between power (pin 8), output (pin 5) and ground (pin 4). There is a slight difference in traces for the output signal between Part A and Part B.

Part B was powered at 3.3V and output monitored with a 10K ohm load. It operated at the specified frequency (14.745M Hz) but the waveform was not a square wave as expected.
Often difficult to distinguish between EOS/EOL (electrical overstress and electrical overload) and ESD. Some rules of thumb:

- **ESD damage**
  - Small failure sites
  - Not always visible without deprocessing
  - No visible evidence at the package level

- **EOS damage**
  - Large areas of damage
  - Burned silicon and metallization
  - Sometime visibly evident package damage
EOS: Thermal overstress to a component’s circuitry

- Short Pulse Width Failure – Junction Spiking
- Long Pulse Width Failures – Melted metallization and open bond wires

Junction spiking occurs when the amount of Al migration into the silicon substrate has reached the point wherein the Al has penetrated deep enough so as to short a p-n junction in its path. By that time an Al spike is said to have shorted the junction, damaging the device permanently.
Images of ESD Damage

Figure 1. ICs with inadequate ESD protection are subject to catastrophic failure—including ruptured passivation, electrothermal migration, splattered aluminum, contact spiking, and dielectric failure. (Image courtesy of Maxim IC)
ESD Failures: Latent Failures

Latent Failures
- ESD events not only impact assembly yields, but also can produce device damage that escapes testing and causes latent failures in the field.
- Devices with latent ESD defects have been referred to as “walking wounded” because they are degraded but still function.
- Latent damage can occur when an ESD event is not sufficiently strong to destroy a device.
  - Device continues to function and is still within data-sheet limits
  - Device can be subjected to numerous weak ESD events, with each new event further degrading a device until total failure
  - No known practical way to screen for walking wounded devices
  - Damage to insulators: weakening of the insulator structures, leading to accelerated breakdown and/or increased leakage
  - Damage to junctions: lowering the lifetime of minority carriers with consequent bipolar transistor gain loss; increasing resistance in forward biased state; increasing leakage in reverse biased state
  - Damage to metallization: weakening of the conductor, leading to increased resistance or increased rate of electromigration
ESD Failure Modes

- Different ESD models tend to produce different types of failure and require different types of control and protection.
- Basic failure mechanisms include:
  - Oxide punchthrough
  - Junction burnout
  - Metallization burnout

Gate-oxide damage to an input buffer after CDM stress. Note the rupture in gate oxide. Image courtesy of TI

Drain-junction damage in an NMOS after HBM stress. Note the thermal damage to silicon. Image courtesy of TI.
Commonly used Failure Analysis Equipment
X-Ray Microscopy

- Digital detector
  - Provides greater contrast through wider range of grayscale (elemental differentiation)
  - Prerequisite for 3-D imaging

- Laminography
  - Provides X-ray sectional images and slice in any direction as well as three-dimensional visualizations of the specimen

- Types of laminography
  - Agilent 5DX
    - Best setup for inline inspection; moderate FA capabilities
  - Everyone else (computed tomography)
    - Allows for ‘virtual cross sectioning’ and 3-D reconstruction
    - Requires rotation of the sample (limited sizing) and extensive exposure time

- Resolution
  - Sub-micron

- Oblique viewing
  - Increases capability of 2-D viewing
  - 60 to 80 degree capability
Scanning Electron Microscopy

- Sample rastered with an electron beam
- Emitted electrons sorted by delay and quantity
Scanning Electron Microscopy

- Secondary electron detection yields topographic information
- Backscattered electron detection also used for topography and elemental analysis
Energy Dispersive X-Ray Spectroscopy (EDS)

- Used with SEM
- X-ray emission signature from electron source
- Elemental analysis of solid samples
- Identification based on multiple emission lines (K, L, M)
- Can’t detect light elements: H, He, Li, Be
- Emission from subsurface “tear drop”

Monte Carlo simulation of Si K-α X-rays in an SiO2 matrix at 5 keV (Vanderlinde, 2004)

EDS scan of elemental copper
Decapsulation

- **Note:** point of no return! Voids any warranties

- **Mechanical preparation and removal**
  - Non-critical material adjacent to die removed with diamond wheel
  - Gross package removal with razor blades, carbide/diamond drill bits, and polishing wheels
  - Stop once the tips of the wirebonds are contacted: electrical testing possible

- **Chemical removal**
  - **Warning:** significant safety precautions and training required
  - Methods: heated sample + dropper application or immersion
  - Fuming nitric acid: apply, rinse in IPA, ultrasonic rinse with methanol
  - Fuming sulfuric acid: apply, ultrasonic rinse in DI water and then methanol

<table>
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<tr>
<th>Material</th>
<th>Nitric</th>
<th>Sulfuric</th>
<th>Dynasolve 160</th>
<th>Uresolve +</th>
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<tr>
<td>Silicone package, gel</td>
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<tr>
<td>Silicone die coating</td>
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</table>

Source: Wills et al., Microelectronics Failure Analysis
Cross-Sectioning

- **Standard method for destructive subsurface evaluation**
- **Method:**
  - Cleaving/sawing to approximate area of interest
  - Potting in epoxy resins to aid polishing
  - Polishing medium dependent upon materials: typically diamond, SiC, or alumina suspensions & embedded polishing cloths
  - Coarse to fine (600 grit to 0.05 um) grinding sequence to eliminate damage from previous step
  - Final etch often used for microstructural relief
  - Optical/electron microscopy techniques used for inspection thereafter
Cross-Sectioning: Chip Front & Backside Polishing

- Used to isolate single IC layers for defect inspection
- Top surface optical/SEM images can be correlated with top or bottom surface thermal/electrical/optical images (see subsequent techniques)
- Special fixtures and CMP methods used for maintaining parallelism

Parallel lapped low k ILD

Lap & plasma ash of underfill
SQUID Microscopy

- Superconducting Quantum Interference Device (SQUID)
- Current flow in devices produce a magnetic field
  - SQUID uses a highly sensitive magnetic detector (superconductor) to resolve these fields
  - Magnetic field image is converted to a current density image, allowing for fault location
- Resolution
  - 500 nA, 300 nm
  - Dependent on working distance (requires a flat sample)
SQUID Microscopy

- Critical technology for detecting package level electrical shorts
  - Much more rapid failure site resolution
  - Absolute confirmation of shorting path
  - Thermal imaging induces damage
Focused Ion Beam (FIB) Microscopy

- Similar to SEM, except that Ga ions are used instead of electrons
- Selective material removal with Ga ion beam
- Excellent for micro- cross sections, electrical circuit isolation, and TEM sample preparation

Source: Hooghan, Microelectronics Failure Analysis, 2004

FIB cross-section of line

Sample removal for high resolution TEM.
Electron Beam Techniques

- Techniques utilize SEM with electrical vacuum feed-through
- Electron beam-induced current (EBIC)
  - Fermi transitions
  - Si defects
- Resistive contrast imaging (RCI)
  - Buried and open conductors
  - Passivated ICs
- Charge-induced voltage alteration (CIVA)
  - Open conductors
  - Passivated and depassivated ICs

Source: Cole, Sandia National Labs, 2004
Optical Beam Techniques

- Techniques utilize SOM (scanning optical microscope) and lasers
- Optical beam-induced current (OBIC)
  - Fermi level mapping
- Light-induced voltage alteration (LIVA)
  - Visible laser on front, IR on back
  - IC defects, logic states, ESD
- Optical beam-induced resistance change (OBIRCH) and thermally-induced voltage alteration (TIVA)
  - IR > 1.1 um (> band gap of Si)
  - Electrical shorts
- Seebeck effect imaging (SEI)
  - Opens

Source: Cole, Sandia National Labs, 2004
Contact Information

- **Questions?**
  - Contact Cheryl Tulkoff, ctulkoff@dfrsolutions.com, 512-913-8624
  - askdfr@dfrsolutions.com
  - www.dfrsolutions.com

- Connect with me in LinkedIn as well!
Your Partner Throughout the Product Life Cycle
Who is DfR Solutions

Key Facts

• Founded in 2005 in College Park, MD

• 20+ Employees
  • Multiple US locations

• Offerings
  • Research, Lab Services, Consulting, Software

• 300+ customers, including:
  • Dell, HP, Apple, Microsoft, IBM, Ericsson, Cisco Systems, Verizon, Huawei, Polycom, AMD, and Nvidia
Focus on Quality/Reliability/Durability of Electronics

Reliability Physics + Commercial Experience + Onsite Laboratory = Unparalleled Results

All levels of the supply chain
Expertise in All Technologies

- Microprocessors
- Chassis
- GPUs
- PCBs
- LCDs
- Fans
- Power Supplies
- Capacitors
- Connectors
- Batteries
- Hard Drives
- LEDs
Our Customers (over 400 and growing)
DfR Solutions – Senior Experts

- Dr. Craig Hillman, CEO and Managing Partner
  - Expertise: Design for Reliability (DfR), Pb-free Transition, Supplier Benchmarking, Passive Components, Printed Circuit Board
  - PhD, Material Science (UCSB)

- Dr. Nathan Blattau, Senior Vice President
  - PhD, Mechanical Eng. (University of Maryland)

- Walt Tomczykowski, Vice President, CRE
  - Expertise: Systems Eng., Life Cycle Management (including obsolescence), Spares Analysis, Counterfeit Mitigation, Failure Analysis
  - M.S., Reliability Eng. (University of Maryland)

- Cheryl Tulkoff, CRE
  - Expertise: Pb-Free Transition, PCB and PCBA Fabrication, IC Fabrication, RCA (8D and Red X)
  - B.S., Mechanical Engineering (Georgia Tech)

- Dr. Ron Wunderlich
  - Expertise: Design for EMI/EMC, Power Supply Design, Analog Circuit Design, Spice Model Development, Monte Carlo Circuit Simulation
  - PhD, Electrical Engineering (SUNY – Binghamton)

- Greg Caswell
  - Expertise: Nanotechnology CMOS, CMOS/SOS, Input Protection Networks / ESD, SMT, Pb-free
  - B.S., Electrical Engineering (Rutgers)

- Dr. Randy Schueller
  - Expertise: IC Fabrication, IC Packaging, Pb-Free Transition Activities, Supplier Benchmarking, Corrosion Mechanisms
  - PhD, Material Science (University of Virginia)

- Dr. Gregg Kittlesen
  - Expertise: LEDs, LCDs, Microprocessors, Memory Components, Photonic and RF Technologies, Supply Chain Management
  - PhD, Analytical Chemistry (MIT)

- James McLeish, CRE
  - Expertise: FMEA, Root-Cause Analysis, Warranty Analysis, Automotive Electronics, Physics of Failure, Battery Technology
  - M.S., Electrical Eng. (Wayne State University)

- Norm Anderson
  - Expertise: Avionics, Product Qualification, Safety Criticality Assessment, FTA, FMEA, Component Uprating, Obsolescence
  - B.S., Electrical Engineering (Iowa State University)

- Anne Marie Neufelder
  - B.S., Systems Engineering (Georgia Tech)
DfR Resources and Equipment

**Electrical**
- Oscilloscopes (Digital and Analog)
- Curve Tracers (Digital and Analog)
- Capacitance Meters
- Low/High Resistance Meters
- High Voltage Power Supplies (Hi-Pot)
- Network Analyzer (up to 3 GHz)

**Testing**
- HALT / HASS
- Temperature Cycling
- Thermal Shock
- Temperature/Humidity
- Vibration
- Mechanical Shock / Drop Tower
- Mixed Flowing Gas
- Salt Spray
- Capacitor Testing (Ripple Current, Step Stress, Partial Discharge)
- Fan Testing
- Bend Testing (Cyclic and Overstress)
- Mechanical Testing

**Material Analysis**
- X-ray
- Acoustic Microscopy
- Infrared Camera
- Metallographic Preparation
- Stereoscope / Optical Microscope
- Scanning Electron Microscope
- Energy Dispersive Spectroscopy
- Ion Chromatography
- FTIR (Solid / Film / Liquid)
- Thermomechanical Analyzer
- Mechanical Testing (Tension, Compression, Shear, etc.)
- SQUID Microscopy

**Other**
- Circuit Simulation
- Finite Element Analysis (FEA)
- Computational Fluid Dynamics
- **Reliability Prediction (Physics of Failure)**
Case Study: New Technologies + Complex Systems

- DfR staff performed reliability evaluations from individual components to entire system

  - Components
    - Quality assessment
    - Lifetime prediction based on physics of failure

  - System
    - Overall reliability
    - Impact of false enforcement on train delay
    - All segments considered [onboard (locomotive), wayside, back office, and communication overlay]
The notion that a transistor ages is a new concept for circuit designers … <sic> engineers traditionally guarantee the transistor will operate for 10 years or so…But as transistors are scaled down further and operated with thinner voltage margins, it’s becoming harder to make those guarantees...
IEEE Spectrum, June 2009

- Developed multi-mechanism solution
  - Designed for the end-user (OEM)

- Value Proposition
  - Tradeoff studies, reliability predictions, system prognostics / self-healing, supplier engagement
Tech Insertion: Tech / Market Benchmarking and Surveys

- DfR uses its unique expertise to benchmark critical technologies and capture risk / current market acceptance
  - Degree of maturity, major suppliers and capabilities, expected costs, quality/reliability concerns

- Technologies recently assessed
  - 0201/01005, System-in-Package (SiP), GaN FETs, Optoelectronics, PCB Platings

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<th>4H-SiC</th>
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<td>Saturated E-Drift Velocity (10E7/cm)</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm-K)</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Thermal Expansion (x10E-6/K)</td>
<td>3.8</td>
<td>4.2</td>
<td>5.6</td>
</tr>
</tbody>
</table>
Design Review: Network Switch

- Manufacturer of network switches wanted to understand potential costs of switch from 3-yr warranty to lifetime warranty

- Identified components that could experience wearout
  - Fans, electrolytic capacitors, integrated circuits, solder joints, plated through holes, ceramic capacitors, connectors, LEDs, overstressed components

- Performed circuit/thermal analysis to identify overstressed components
  - Especially based on usage model (validated through internal DfR testing)

- Predicted reliability for each component based on validated algorithms
  - Primarily conducted through Sherlock™
  - Conducted component testing when necessary
Design Review: Power Amplifier

- Component manufacturer pushing the limits to increase market share
  - Driving RF CMOS transistors beyond foundry’s specification
  - New packaging technologies (copper pillar, copper wirebond, low Tg underfill)

- Comprehensive assessment
  - Initial transistor life prediction
  - Finite modeling for prediction of 1\textsuperscript{st} and 2\textsuperscript{nd} level lifetime
  - Guidance on qualification plan
Case Study: Supplier Assessment/Audit

Going Beyond ISO 9001

Problem:
- Improve Quality
- Manage Suppliers

Approach:
- Guidance from DfR

Solution:
- Documents, Onsite Audits, Training

DfR Solutions
Supplier Assessment: Fans

- Developed internal capability based on strong market need
- Unique environmental chamber
  - Elevated temperature with power cycling
  - Fan loading through pressure differentials
  - Multiple failure detection techniques (sound, current draw, rotational velocity)
  - Up to 200 fans
- Develop accelerated technique based on knowledge of fan failure mechanism and degradation algorithms
Case Study: Test Plan Development

Developed and executed test plan based on physics of failure
Testing: Next Generation Microprocessor

- Selected as the preferred vendor for package qualification testing
  - Reviewed coupon designed, identified deficiencies

- Tests performed
  - Nine point cyclic bend
  - Static bend
  - Drop
  - Mechanical shock
  - Harmonic vibration
  - Random vibration
  - Thermal cycling
  - Temperature / humidity
The number one requirement in failure analysis

DfR has all the necessary elements
- Electrical engineers, mechanical engineers, materials scientists, inorganic chemists, etc.

Extensive in-house expertise
- PhD, MS, BS + industry experience

The right background
- Over 1000 failure analyses combined
Root Cause Analysis: Desktop Computer

- Failures during HALT
  - Exposure to vibration
- Electrical testing indicated electrical open
  - Under BGA socket
- Validity of failure mechanism?
  - Shearing of electrolytic capacitor leads
- Dependent upon orientation of capacitors
  - Only those along the board length
- Vibration test may not have applied random loads
  - Potential issues with vibration table or fixturing
Let your staff learn all day / every day

E-LEARNING

- Scholarly articles
- Technical white papers
- Case studies
- Reliability calculators
- Online presentations
Interested?

- Could your next product benefit from DfR’s extensive expertise and PoF knowledge base?
  - Bring us in as an independent party during critical design reviews

- Are your concerned with new technologies?
  - DfR’s scientists and engineers can provide comprehensive analysis to ensure risk-minimization during these difficult transitions

- Take advantage of our unique Open-Door policy!
  - See how much we already know about your current issues
  - Chances are we have already solved your problem at least once before
  - We work around the clock and around the world
  - Contact us by phone (301-474-0607) or email (askdfr@dfrsolutions.com)