Avoiding the Pitfalls of Voiding in PCB Assemblies

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Overview

I. What is Voiding
   i. Causes
   ii. Concerns
   iii. Types of Voiding

II. Bottom Termination Components
    i. What are they? Why do we use them?
    ii. Sources of Failure
    iii. Analysis

I. Key Factors to Consider
   i. Symptom or Defect
   ii. Tackling Assembly Challenges

II. Design for Success
    i. Reflow Profile
    ii. Preforms
    iii. Achieving the Lowest Level of Voiding

III. Summary
Causes

These voids are generated from:

- Volatiles Outgassing
- Non-Wetting
- Solder Starvation
Potential Factors Affecting Voiding
When is it a Concern?

- Mechanical Reliability
- Electrical Efficiency
- Thermal Transfer for High Power Applications
- Solder Bridging for Fine Pitch
Types of Voiding

- Macro Voids
- Planar Microvoids
- Shrinkage Voids
- Intermetallic Microvoids
- Pinhole Microvoids
- Micro-Via Voids


Intel Corporation presentation on “Voids in Solder Joints” from SMTA Boise on March 20th
BTCs
What and Why?

- Low cost/ Easy to make
- Ideal for miniaturization
- Reduced lead inductance
- Mechanically robust due to flat terminations located underneath the component body
- Standoff determined by solder volume
- Voiding induced from stand-off height and size of pad
BTCs
Sources of Failure

1. Shorted or missing I/O connections due to fine pitch or small area ratio
2. Insufficient standoff height or tilt
3. Excessive voiding

Hot Spots
BTCs

X-ray Analysis

• **Contrast denotes density!!**

• Numerical outputs:
  – Overall voiding % in 2-D
  – Largest void size in 2-D
  – # of voids in 2-D

• Watch for inconsistent appearance on perimeter solder joints

• Must also consider standoff height as it relates to number of voiding (in 3-D or CT X-Ray or in a cross section)
Key Factors to Consider
Symptom or defect?

- **Void percent**
  - How much voiding can *your* solder joint handle?
  - Application-specific

- **Position of void important**
  - Close to the interfaces (z-axis)
  - Under die, prohibiting thermal dissipation
  - Center vs. Edges

- **Solder joint reliability may be compromised from combination of voiding plus low stand-off height (Check both)**
Key Factors to Consider Tackling Assembly Challenges

Goals:
- “Low” voiding
- Consistent (sufficient) standoff height
- No tilt
- No bridging on perimeter IOs
Design for Success
BTC Pad

• To via or not to via…
• Via design?
• *Pay close attention to the recommendations for the specific component you use*
  – Thermal dissipation
  – High power requirements
  – Soldered thermal pad?
• Solder mask patterning?
• Stencil design
Design For Success
Stencil Design: Case Study

4 mil and 5 mil laser-cut

Nine squares, fine pane
Full pad print
Quadrants, fine pane
Quadrants, wide pane

Conclusion: The amount of paste volume is not directly related to the amount of voiding percent.

From “How Stencil Design and Reflow Profiles Affect Variation in QFN Voiding Data: A Case Study” SMTA ICSR 2016
Stencil Design Outcomes

- Stencil design doesn’t fix voiding but may limit variation
- Start with designing appropriate perimeter deposits
- Add minimal pane in center deposit to discourage component float during reflow
- Don’t sacrifice solder volume unless there’s good reason
- Avoid printing paste over vias
- Mind the placement step, components may squish venting channels
- Pre-reflow standoff height is key for outgassing
Design for Success
Reflow Pitfalls to Avoid

• Ramp slope too quick:
  – Not enough time to outgas before liquidus
  – Paste slumps, reducing standoff for volatile escape
• Profile too short:
  – Not enough time for alloy to wet to the surface
  – Inconsistent outgassing

• Low peak temperature:
  – Could reduce wetting (varies dependent on alloy)
• Excessive peak temperature or profile length:
  – Oxidation on surfaces
  – Increased risk for other reflow defects
Design for Success
Reflow Profile – No Magic Bullet
Design for Success
Reflow Pitfalls to Avoid

- Profile with a populated board!!
- TC attachment
  - Drill under BTC’s
  - High Temp Solder/Aluminum Tape/Conductive Epoxy
  - “window-pane” thermal tape with Kapton
- TC’s on the **solder joint**, not on the component
Design for Success

Preforms

- Flux-less or low-flux coating
- Ratio of solder to flux to reduce voiding percentage
- Remedy voiding due to solder starvation
- Increase volume of solder to raise stand-off height

From: “Voiding Controls Beneath BTCs Using Solder Fortification® Preforms”

From: “The Benefits of Flux-Coated Preforms in a QFN Assembly Process”
Design for Success
Standoff Height After Reflow

Perimeter solder squished out

Proper perimeter solder joint

0.3mm Vias

0.2mm Vias with FC Preform
Design for Success
Achieve Lowest Level of Voiding

Use preforms with solder paste:

• Overcome non-ideal design points by adding solid solder preforms
  – Square, thin, flux-coated preforms in center pad
  – Solder Fortification® (0402s or 0603s)

• Alternative reflow processes:
  – Vapor phase
  – Vacuum reflow
Summary

- Voiding may not always be a concern
- BTCs offer advantages over other leaded components but promote voiding
- Stand-off height is important to consider
- Avoid printing paste over vias
- Stencil Design may reduce variation in voiding
- Reflow profile does not need to be complex
- Preforms and other reflow methods offer lowest voiding
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