Advanced Packaging For Mobile and Growth Products

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Growing Needs for Silicon & Package Integration

New converged applications require more complex & customized packaging solutions

Converged Market

Mobile Computing

Convergent Products

US$28.8B
37.5% CAGR

Communication

US$125.4B - 2010
US$136.1B – 2013
2.8% CAGR

US$70.3B - 2010
US$80.9B – 2013
4.8% CAGR

Packaging Trend

2D SoC

QFN, FBGA, fcBGA, fcFBGA, eWLB, WLCSP

3D SIP

PoP/PiP, FBGA-SD, ISM, Module

3D IC

F/BGA-TSV-SD, PoP-TSV, eWLB, IPD

Implication to OSAT

• Pressure on packaging cost
• Needs for best valued BOM
• More flip chip & WLP (capital intensive)
• Yield & cycle time

• Die thinning & stacking
• Advanced multi-tiers wire bonding
• Passives discrete handling or IPD
• Yield & cycle time

• Capital intensive
• Silicon interface know-how
• 2.5D IC using Si interposer
• Yield & cycle time

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Heterogeneous integration; advanced 3D PKG solutions

- CMOS IC to 22nm & Beyond
- IC & 3D Module & 3D IC Pkg: eWLB/Fanout Wafer Level PKG
- 3D IC Systems with TSV
Drivers for Mobile /Portable Device Packaging

- Size (area and thickness)
- Performance
- Cost
- Standardized
- Reliability
- Environmental
More and More WLCSPs in mobile phones

WLCSP (wafer level CSP)
• Many Billions of Packages Shipped
• Established worldwide Industry Infrastructure
• Lead free & MSL1
• I/O ranging 12 - 144

Smart Phone WLCSP Statistics
• Apple iPhone 48 dies - 21% are WLCSP
• RIM Blackberry Storm 42 dies - 29% are WLCSP
• Nokia 95 50 dies - 50% are WLCSP
Advanced Wafer Level Integration Technology Evolution

LEADED PACKAGING

ARRAY PACKAGING

EMBEDDED & 3D PACKAGING
- Advanced node compatibility
- Large Scale
- Low cost
- Higher integration
- Performance
- Reliability
- Design Flexibility

eWLB

3D TSV ICs

TSV Interposer

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Evolu&on of 3D Packages

Integration, Density, Performance

Stacked Die

(24 die-stack)

Stacked Packages
PoP (eWLB) & PiP

TSV stacked 8G DDR3, 2011

Ultra low proﬁle eWLB+MLP

3D eWLB

Development

Production

Manufacturing Maturity

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Portable/Mobile Electronics- Package Trends

- Stacked Die Packages
- Package on Package (PoP)
- eWLB / FO-WLP / EDS
- Through Silicon Vias (TSV)

3D Chip Packaging Solutions
- SiP–System in package
- SoP–System on package *(High Density Heterogeneous / Modular Chips Integration)*
- SoC–System on chip *(Single Chip- Chip Level Integration)*
- Chip packaging compatibility with SMT assembly process
- 3S Reliability
- 3S Assembly process, material and rework
Silicon Interposer Delivers High Interconnect Density
eWLB and Wafer Level Packaging Technology
Driving Forces to Wafer Level Package

Cost
- Packaging cost
- Test cost

Dimensions
- Package height (↓)
- Lateral dimensions (↓)

I/O Density
- Pitches (↓)
- No standards
- Small chips/high no. of I/Os

Functionality (Integration)
- Integrated Passives (R, L, C)
- System in Package
- 3D

Wafer Level Packages
- Batch processing
- High parallelism
- Improved test concepts
- Smallest package heights
- Minimum lateral area

Electrical Performance
- Interconnect line length (↓)
- Operating frequencies (↑)
- Package Speed (↑)
- Parasitics

Thermal Performance
- Power consumption (↑)
- Package Density (↑)

- Min line length
- Multilayer RDL
- Reduced no. of interconnects

- Integrated passives in RDL
- SiP/3D capability
- Improved chip to board coupling

- Min pitches
- Improved chip to board coupling
What is eWLB?

- A new Wafer Level Packaging technology, utilizes well developed wafer bumping infrastructure, with an innovative wafer reconstitution process to package Known Good Dice.
- Wafer level package, uses mold compound to support the fan-out I/Os.

**Fan-In WLP**
PKG size = Chip size

- Fan-In Interconnects only - Number and pitch of Interconnects must be adapted to the chip size
- Only Single chip packaging solution

**eWLB/Fan-Out WLP**
PKG size > Chip size

- Fan-out Interconnects - #, Pitch of Interconnect is INDEPENDENT of chip size
- Single/Multi/3D chip packaging solution
- Improved Yield with KGD

eWLB expands the application space for Wafer Level Packaging!
Advantages of eWLB Technology

- Thinner & smaller package solution
  - Ideal for mobile applications and meeting future roadmaps
- Package robustness (vs. LF flip chip + advanced fab nodes with ELK)
  - Cu/ELK compatible packaging technology (65nm in HVM, 40nm in Qualification)
  - Green packaging (Generic Pb-free, Halogen free)
- Superior board level reliability proven for mobile applications
- Proven lower cost path using a batch process & simpler supply chain
- Next generation eWLB technology with 3D eWLB joint development
- No substrate or bumping; Simple logistics and supply chain
**eWLB Products Portfolio**

- **Single chip eWLB**
- **Multi-chip eWLB**
- **2.5D / Extended eWLB**
- **3D eWLB**
- **eWLB-MLP**
Next Generation eWLB

10mm/10mm line width and line spacing

Thin packaging solution (<0.5mm)

Plated Cu RDL

for more design and routing flexibility

250mm thin eWLB

Embedded Passives

3D (double-side) eWLB

Multi-die eWLB

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Multi-Die eWLB (Side-by-side)

3-die eWLB
- PKG: 12x12sqmm, 0.5mm ball pitch
- Die: 3-die, 2 (3x3mm + 3x4mm)
- I/O Count: 396
- 1-L RDL

2-die eWLB
- PKG: 12x12sqmm, 0.4mm ball pitch
- Die: 4x4mm (2 dies)
- I/O Count: 580
- 2-L RDL

Reliability Test | Pre-condition | Test Condition | Read-out | Pass
---|---|---|---|---
Multiple Reflow | - | LF bumps @ 260 °C | 5x, 10x, 20x | √ passed
Unbiased HAST | MSL1 | 130°C, 85%RH | 96hr | √ passed
Temperature Cycling | MSL1 | -55°C/125°C (G) | 500x, 850x | √ passed
High Temp. Storage | MSL1 | 150°C | 500, 1000hr | √ passed
TCoB | -40/125C | 500x | √ passed
Drop test | Nokia Spec | - | √ passed

Highly integrated SiP or side-by-side packaging solution with multi-die. Can be integrated with IPD, RDL passives or discrete MLCCs.
Double-side 3D eWLB

Package Specification
• PKG: 12x12sqmm, 0.5mm ball pitch
• Die: 3-die, 2 (3x3mm) + 3x4mm)
• I/O Count: 396
• 1-L RDL (Top and Bottom both)
• Thickness 450um / 250um

 Passed JEDEC component level and board level reliability tests

Low profile 3D eWLB PoP (12x12mm PoP-bottom package) with less than 1mm thickness including solder balls.

Picture of 3D eWLB PoP packages; Total less than 1.0 mm package height (including solder balls)
Ultra Low Profile eWLB PoP: eWLB-MLP (embedded Wafer level Molded Laser PoP)

- Thin POP (250um pkg body thickness)
- Low warpage during solder reflow cycles
- Larger Si die cavity
- Flexibility in memory interface
- High routing density: L/S=10/10 (um)
- Compatible with ELK
- Good thermal performance
  - $Q_{JA} \ 18-22(\degree C/W)$
  - $Q_{JB} \ 3-7(\degree C/W)$ for 12x12mm eWMLP)
eWLB : Thermo-Moire, High Temperature Warpage Measurement

[Graph showing warpage vs. temperature for fcBGA and eWLB]

fcVFBGA, 7x7mm, 191LD NSP
PKG height 0.95 mm
Die 4.46 x 5.65 x 0.19 mm

[Diagram of fcVFBGA]

eWLB 8x8mm, 182I/O
PKG height 0.7 mm
Die 5 x 5 x 0.45 mm

[Diagram of eWLB]
TSV Technology
• 3D IC TSV
• 2.5D Interposer
TSV Technology for mobile devices (Logic + Memory) - Wide I/O memory interface in mobile
- Examples: AP+DRAM or AP/BB combo+DRAM in mobile devices

• High Performance Devices
  - High electrical performance solution: Increasing number of I/Os
  - Power effective solution: Minimized output loading with CtC connection
  - TSV for shorter interconnection length for better performance
  - Micro-bump
  - Micro-bump bonding (50/40um pitch): Thermal Compression with NCP

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Lower cost (High yield) & higher performance

For embedded memory;
- Nominal LSI Memory capacity ↑ 2X per node
- eDRAM shrinks < 40% per node
- Total memory area grows node to node

De-couple functional blocks in SoC (analogue, memory, I/O, RF,...)
- Heterogeneous integration in Pkg
Thermo-compression Bonding
- Thermo-compression Bonding (TCB) of 40um pitch with Cu column and NCP (non-conductive paste)

Chip-to-Chip

40/50um pad pitch with ENIG pad finish on Cu pad

Chip-to-Substrate

40um pitch Cu column on Substrate

No void observed after TCB with NCP)
TSV Silicon Interposer (TSI) Technology

*Provide High Complexity, High Performance ASICs with Dependable Predictability*

**Technology Disaggregation**

- Optimization of Silicon Technology for Individual IP
- Higher Levels of System Integration
- Wider Product Capability Offering to Customers
- Lower Total System Power
TSV Silicon Interposer (TSI) Technology - Continued

External Memory Solutions
\- Increase Memory Options for Customers
\- Increase Memory Storage per ASIC
\- Low Power and Higher Bandwidth
\- Leverage Industry Standard Memories

Die Separation
\- Decrease Yield Losses of Large Die
\- Decrease Yield Losses Early in
Functional Partitioning with TSI

Heterogeneous Integration
- Silicon interposer advantages
  - Reduced die complexity
  - Mixed technologies

2.5D TSV interposer

Source: Xilinx 2.5D FPGA
2.5D and 3D will Coexist?

- 3D especially with TSVs is a revolutionary change requiring significant infrastructure additions.
- 2.5D allows use of mixed interconnect ICs from different sources and is evolutionary.
- 2.5D may become as essential within a package assembly as underfill epoxy for both single chips and stacked 3D chips.
- 2.5D is not limited to silicon - glass and even organic solutions provide economical benefits in applications where silicon is inappropriate.
Summary

- Wafer level packaging is a key technology enabler for future heterogeneous integration.

- Next generation and 3D eWLBs would be a good solution for future needs in mobile/portable applications, such as PoP and 3D SiP.

- With scale-up and higher throughput, large panel approach is next step for further market-penetration as cost-effective packaging solutions.

- TSV technology is critical for continued evolution of semiconductor industry. TSV interposer technology is one of early application of TSV technology.

- As with all new technologies for 2.5D/3D TSV wafer level integration; Product applications & drivers are critical.

- Alternative technology, eWLB technology, wafer level packaging solution enabling 3D wafer level integration with low cost solution.

- More collaborative cost/ performance analysis across FE-BE FAB, EDA, Assembly, Reliability, Metrology & Test are needed for successful TSV biz establishment.
Thank You