Agenda

1. Types of Flying Probe systems
2. Application of Flying Probers
3. PCBA physical limits & requirements
4. Test Access
5. Test Program Methodology
6. Complementary technologies integration
Types of Flying Probers

A. First Generation FP – starting mid 1990s in N.A.
   • Single Sided with flying probes on the top side only
   • Four angled Flying Probes on top side
   • Manually placed (Fixed) Probes on bottom side

B. Second Generation FP – starting mid 2000s in N.A.
   • Double Sided with angled flying probes on the top and bottom side
   • Four angled Flying Probes on top side
   • Two Flying Probes on bottom side

C. Third Generation FP – two suppliers W.W.
   • Double Sided with flying probes on the top and bottom side
   • Four or more Flying Probes on top side
   • Four or more Flying Probes on bottom side
   • Incorporate complementary technologies such as Boundary Scan, Thermal…

D. Other FP types
   • One and/or two Flying probes from one side for diagnosing defects
   • Backplane testing using connectors
   • Bareboard Flying Probers for testing bare PCBs without components
Applications of Flying Probers

- New PCBAs for NPI, prototype and low volume testing
- Connector testing
- Backplane testing
- Field returns
- Reverse Engineering
- Battery
- Continuity (Link) testing
- Substrate testing
- Load Board testing
- Fault Injection
- Copper plating measurement
- Wafer testing
Flying Prober Selection Factors

1. PCBA Volume - FP best suited for low-volume/high-mix production environment
2. Test Access - FP best solution when electrical test is required and insufficient ICT test access (18mil+) is not available
3. Deployment Time - FP best solution when test window is limited to a few hours or a few days
4. Changing PCB Layout - best solution when the PCB layout can be revised such as prototype, NPI and short runs
5. Non Traditional Applications - testing of substrates, connectors, and other electrical cases
Low Volume/High Mix Usage Model

Strategy: highest test coverage within delivery time constraint.

- Includes NPI, Prototypes, first articles and evaluation boards.
- Other Test & Inspection Technologies: SPI, AOI and HVI
- Development time: 1 to 16 hours (offline)
- Debug time: 4 to 16 hours
- Segment: EMS & OEM
- Functional test at OEM
- Batch Testing
- Industries: Mil/Aero, Industrial, Server, Telecom ...
Repair/Rework Usage Model

Strategy: highest test coverage.

- Low volumes
- Other Test & Inspection Technologies: SPI, AOI, AXI, ICT(programming) and HVI
- Development time: 1 to 16 hours (offline)
- Debug time: 4 to 40 hours
- Segment: OEM
- Functional test at OEM
- Batch Testing
- Industries: Mil/Aero, Industrial, Server, Telecom ...
Selective/Sample Usage Model

Strategy: highest test coverage within line beat rate. Typically test first board 100% and then verify any line changes

- High volume such as automotive boards.
- Other Test & Inspection Technologies: SPI, AOI, AXI, ICT(programming) and HVI
- Development time: 1 to 16 hours (offline)
- Debug time: 4 to 32 hours
- Segment: OEM
- Functional test at OEM
- Inline Testing
PCBA Loading Issues - Conveyors

- Edge Clearance on two Parallel sides of the UUT are required – 3 mm
- Best along the longest edges of the UUT to prevent sag
- Predictable leading edge dimension required for board stopping position on systems with automatic conveyors

In the case with odd shaped boards two solutions exist:
- Use break away rails that comply with the above
- Use a custom or universal carrier to move the UUT into the machine.
PCBA Alignment and Fiducials

3 Board FID points are required on both top and bottom of the UUT

- Placed near the perimeter of the UUT
- Must be free from solder after production
- Must not be identical from top to bottom
- Must not be near similar graphics, etches, silk screens.
- Must be clear from the 3mm edge clearance
- Should be in the CAD as a part or easily identifiable entity.
According to the IPC-SMEMA Council Fiducial Locating marks should have the following characteristics:

- Size: 1 mm to 3 mm in diameter (40 – 118 mils)
- Clearance Area around the FID: 1-2 times the radius of the size

Some samples are below, most commonly used is the circle in circular clearance area.
PCBA Physical Limits

As robotic systems, flying probe machines need to move over parts to go from place to place. Given that they are to contact the board under test and they are not infinitely high from the surface of the UUT. Mechanical limits exist depending on the system you have, or plan to use:

- Fly over heights ranges up to 45mm
- Fly around heights ranges up to 85mm
- Different top and bottom height restrictions
- Test prior to tall part placement
- Weight up to 25 lb. (12Kg)
- Size up to 25” by 39”
- Component shadows
Goal is physical flying probe access to every net on the board.

1. **Dedicated Test Points** - specifically meant for test access
2. **Through Hole Pins as Test Points**
3. **Via Holes as Test Points** – standard or blind but not buried or masked
4. **Surface Mount Pads as Test Points**
5. **Virtual Test Points**
6. **One access point per unconnected net??**

**DO NOT PROBE ON DEVICES LEADS DUE TO POTENTIAL DAMAGE**
TYPICAL 0402 LAND PATTERN

20 mils  43 mils  20 mils

24 mils

31 mils  20 mils  31 mils

Probe target

drawing not to scale
**Probing Error**

**Causes:**
- PCB Production tolerances
- Fiducial recognition
- Steep probe angle
- Conveyors
- Mechanical calibration tolerances
- Different heads

<table>
<thead>
<tr>
<th>Probe Angle</th>
<th>Tangent</th>
<th>Shadow</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>1</td>
<td>0.017</td>
<td>0.244</td>
</tr>
<tr>
<td>2</td>
<td>0.035</td>
<td>0.489</td>
</tr>
<tr>
<td>3</td>
<td>0.052</td>
<td>0.734</td>
</tr>
<tr>
<td>4</td>
<td>0.070</td>
<td>0.979</td>
</tr>
<tr>
<td>5</td>
<td>0.087</td>
<td>1.225</td>
</tr>
<tr>
<td>6</td>
<td>0.105</td>
<td>1.471</td>
</tr>
<tr>
<td>15</td>
<td>0.268</td>
<td>3.751</td>
</tr>
<tr>
<td>16</td>
<td>0.287</td>
<td>4.014</td>
</tr>
</tbody>
</table>

*10 mil high device

Device under test

PCB Warpage

Reference Plane

Outer Probes (1) 0-6/15/16°

Inner Probes (2) 0-6/5/6°

Outer Probes (1) 0-6/15/16°

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# Opens Testing Technology

<table>
<thead>
<tr>
<th>Defects</th>
<th>Diode</th>
<th>Sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opens on ICs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Opens on BGAs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Opens on BGAs with a metal cap or heat sink</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Opens on connectors</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Opens on BGAs with grounded metal cap or</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>grounded heat sink</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polarized caps</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ICs on buses</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>IC w/o Chip Select pin</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Diode Method**

![Diode Method Diagram](image-url)
Opens Testing – Sensors Method

1) Probe acts as a transmitter – sending an RF signal

2) Other Probes Detect & Measure the signal quality for Pass/Fail. This is used on leads, BGA’s and connectors for Opens/Shorts.
Optical Inspection

- 1 camera Top side

- 1 camera Bottom side

OPTICAL CAPABILITIES
- Fiducials
- Reading 1D & 2D barcodes
- Component Presence
- Component Absence
- Component Skew
- Component Part Markings
- No Solder Inspection
Test Program Methodology

1. Shorts testing - not practical to test every net against every other net
   • Adjacent pins technique
   • Geographical distance as defined by the user
   • Selective nets such as power and/or ground to other nets
   • Net impedance learned from a golden PCBA

2. Passive Component electrical testing
   • BOM method – BOM value + device tolerance + system tolerance
   • AutoLearn method – learned golden board + user tolerance

3. Active Component electrical testing

4. Opens testing (Vectorless)
   • IC pins except for power and ground
   • Connector pins if accessible to sensor

5. Optical test
   • Presence, absence, skew and markings of device not electrically testable

6. Power On testing

7. Voltage, currents and other technologies
Different supplier may offer combinations of these options:

- Boundary Scan (Basic & Advanced)
- Laser mapping
- Microscopy
- Bed-Of-Nails
- Device Programming
- Thermal measurement
- External instrumentation integration
Incorporating Boundary Scan Test

- PCBA Power can be provided via probes or external supply
- Boundary Scan controller applies vectors via DUTs’ JTAG port
- Unused probes can monitor internal net for additional test coverage
- Redundant tests can be removed
- Automated test optimization and coverage report generation
Incorporating Flying Bed-of-Nails

Mobile head that carries a Bed of Nails (BON) designed for a fixed pin pattern. BON carry power and/or fixed channels.
# Boundary Scan vs Flying Prober vs ICT

<table>
<thead>
<tr>
<th>TEST TECHNIQUE</th>
<th>BS</th>
<th>PON FP-DS</th>
<th>ICT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorts</td>
<td></td>
<td></td>
<td></td>
<td>Non BS nets; FP slowest; ICT needs access</td>
</tr>
<tr>
<td>Opens</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Passives</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bypass caps</td>
<td></td>
<td></td>
<td></td>
<td>Vision option on FP</td>
</tr>
<tr>
<td>Low value RLC</td>
<td></td>
<td></td>
<td></td>
<td>FP has dedicated hardware</td>
</tr>
<tr>
<td>Actives</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Markings/Barcode</td>
<td></td>
<td></td>
<td></td>
<td>FP has AOI</td>
</tr>
<tr>
<td>Switches</td>
<td></td>
<td></td>
<td></td>
<td>Mechanical contact</td>
</tr>
<tr>
<td>Connectors</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LED colors</td>
<td></td>
<td></td>
<td></td>
<td>ICT fixture sensor</td>
</tr>
<tr>
<td>IC Opens</td>
<td></td>
<td></td>
<td></td>
<td>Vectorless testing (TestJet, FrameScan…)</td>
</tr>
<tr>
<td>Frequency Test</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Test</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC Internal Logic</td>
<td></td>
<td></td>
<td></td>
<td>Using BS</td>
</tr>
<tr>
<td>Device Programming</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Access</td>
<td></td>
<td></td>
<td></td>
<td>BS port; FP 4-8mil; ICT 18-25mil</td>
</tr>
<tr>
<td>Test Fixture Costs</td>
<td></td>
<td></td>
<td></td>
<td>ICT fixture $5-$50K</td>
</tr>
<tr>
<td>Development time</td>
<td></td>
<td></td>
<td></td>
<td>ICT fixture</td>
</tr>
<tr>
<td>Test time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**BS**: Boundary Scan; **DS**: Double Sided; **FP**: Flying Prober

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What the future holds???

- Faster testing
- Smaller test targets
- Incorporating complementary technologies
- Industry specific solutions
- Growing usage