Laminate Based Fan-Out Embedded Die Technologies: The Other Option

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Paper Outline

- Industry Trends in Embedded Die Packaging
- Evolution of Wafer Level Fan-Out Technologies
- Representative Laminate Embedded Die Flow
- Wafer Level vs. Laminate Options (Pros and Cons)
- Laminate Embedded Die Logistics
- Advantages of RDL for Embedded Die Applications
- Laminate Embedded Die Semiconductor Packaging
- Conclusions
Current and Future 3D Packaging Options
Fan-Out WLCSP Packaging Enables Larger Array Sizes

(Yole Developpement)
Wafer Level Fan-Out
Embedded Die Packaging

“Cell Phone in a Package”

Challenges:
- Cost Considerations
- Managing Complexity
- Individual Component Yields
- Cumulative Yield Effects
- Logistical Considerations
- 3D Limitations

Freescale Redistribution Chip Package (RCP™)
Infineon EWLB
Fan-out Technology

Managed Expectations: (Near Term)
- Managing Complexity
- Cost$
- Competing Pkg Alternatives
- Individual Component Yields
- Cumulative Yield Effects
- Logistical Considerations
- 3D Limitations

Reconstructed Wafer Based
Fan-Out Technology
Imbera Embedded Die
Process Sequence

1) Component placement with non-conductive paste attach to pre-patterned Cu foil (alignment marks and laser vias).

2) Lamination of standard glass reinforced, pre-prepreg for dimensional stability.

3) Cu foil patterning to realize the PCB routing layers

4) Typical laminate structures are 2 to 6 layers with more complex structures being up to 10 metal layers.
# Comparison of Wafer Level and Laminate Embedded Die Options

<table>
<thead>
<tr>
<th>Feature</th>
<th>Wafer Level Option</th>
<th>Laminate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Panel / Substrate Size</strong></td>
<td>200 mm Wafer (31.4K mm²) 300 mm Wafer (70.7K mm²)</td>
<td>18&quot; x 24&quot; (0.457 m x 0.61 m) (278.8K mm²)</td>
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<tr>
<td><strong>Infrastructure Availability</strong></td>
<td>- 2010 (Current) ++</td>
<td>- 2012 (Future) +</td>
</tr>
<tr>
<td><strong>Localized Density</strong></td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>- Redistribution Layers</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>- Laminate Layers</td>
<td>N/A</td>
<td>++</td>
</tr>
<tr>
<td><strong>X,Y Routing Density</strong></td>
<td>+++</td>
<td>++</td>
</tr>
<tr>
<td><strong>3D Extendability</strong></td>
<td>+</td>
<td>+++</td>
</tr>
<tr>
<td><strong>In-Process Testability</strong></td>
<td>++</td>
<td>+++</td>
</tr>
<tr>
<td><strong>Yieldability</strong></td>
<td>++</td>
<td>+++</td>
</tr>
<tr>
<td><strong>Cost Effectiveness</strong></td>
<td>++</td>
<td>+++</td>
</tr>
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Laminate based embedded die packaging options will ultimately become the alternative of choice!
Laminate Embedded Die: New Logistics

- Embedded Die Redistribution
  - Wafer Thinning / Stress Relief
  - Wafer Sort / Die Preparation
    - Component Embedding and Core Manufacturing
    - Embedded Die PCB AOI / Sort
  - Multi-Layer Build Up Fabrication
- SiP Back-End (SMT, Molding, Chip Attach)
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Imbera/FCI Embedded Die Work Share
Laminate Embedded Die: New Logistics

Embedded Die Redistribution

Wafer Thinning / Stress Relief

Wafer Sort / Die Preparation

Component Embedding and Core Manufacturing

Typical Short Term Embedded Die Work Share

SiP Back-End (SMT, Molding, Chip Attach)

Embedded Die PCB AOI / Sort

Multi-Layer Build Up Fabrication
Embedded Die RDL Structures
Flexible RDL Design/Fabrication
Fan-In Wafer Level RDL for Ease of Die Embedding

1) Eases large panel die placement requirements.
2) Relaxes laser via tolerance requirements.
3) Lowest cost option for finest interconnects (highest density).
4) Provides corrosion barrier for embedded integrated circuits.
5) Higher overall yields!!
EDC1 Daisy Chain Test Die

Family of standardized daisy chain devices to accelerate the emergence of a robust infrastructure to support embedded die technologies.

- Base substrate: Silicon dioxide wafer
- Die dimension: 6.6 mm x 7.1 mm
- Pitch: 0.15, 0.20, 0.3, 0.4 mm
- Pad on I/O and RDL Versions
- 4 mm x 4 mm and 8 mm x 8 mm

Full Array

4 daisy chain test vehicles
(Die Size: 4 mm x 4 mm and 8 mm x 8 mm)

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Optical Cross-section of a Laminate Embedded Cell Phone Board

(NXP/FCI, 2009 IWLPC)
Laminate Embedded Die Interconnection

Blind Via Down to Ruggedized RDL Pad (x-section)

Plated Cu RDL Pad
Embedded Die QFN

iQFN (Integrated QFN) Features:

1) Plated Cu RDL or pad on I/O as required
2) 1 PCB copper layer enables:
   • Routing requirements of low I/O applications
   • Thin Package Profile (approx. 0.4 mm)
   • Efficient thermal solution in the middle area of the Substrate.
Embedded Die Fan-Out Packaging

Features:

• Enables larger solder ball pitches resulting in lower cost substrates.
• Supports end users with a broad range of SMT assembly capability
• Enables incremental embedded die technology adoption
• Minimal Layer Count
• Highest Density interconnect is completed and Known Good Die status confirmed before embedding => Improved Yields and Costs!
Laminate Embedded Component SiP Solutions

- Managed complexity
- Incremental Complexity gains

Integrated Passive Devices / Integrated circuits

Integrated Discrete Passive Device
Key 3D Enablers of Laminate Embedded Die Packaging Technologies

1 - Dimensional Stability of Glass Reinforced Core
2 - Substrate Core Routability
3 - Z-Axis Interconnectability
4 - 3D Die Stacking Options
5 - 3D Package Stacking Capability
6 - Thermal Solutions
Embedded Die SiP Packaging Solution

Overmolded Wire-Bonded Device

Embedded Die SiP Substrate

Embedded Die is within SiP
Embedded die is on the order of 100 to 150 microns thick.
Example of Embedded Die 3D Package Stacking Applications

Stackable iBGA
Conclusions

- Laminate Embedded Die / FOWLP solutions are emerging.
- FOWLP technologies are enjoying an early lead in embedded die application positioning.
- More complicated logistics for laminate based embedded die solutions are delaying near term technology adoption.
- Technical advantages (2D, 3D) and overwhelming PCB infrastructure will ultimately make laminate options the dominant option.