Industry 4.0 – ASTER Software Suite
Within the modular structured smart factories, cyber-physical systems monitor physical processes, create a virtual copy of the physical world and make decentralized decisions.

✓ Interoperability: Connect machines, devices, sensors and people to communicate with each other.

✓ Digital Simulation: Create a virtual copy of the physical world. Play with “What-if” scenarios in the virtual word in order to identify the optimized physical flow. Use theoretical results to control the physical world.

✓ Convert data into information: Aggregate raw data from cyber-physical systems to build and visualize comprehensive information that allow humans to make decisions based on facts.

✓ Decentralized decisions: the ability of cyber physical systems to make decisions on their own and to perform their tasks as autonomously as possible.
Enhanced Manufacturing Services 4.0

Traditional Workflow: Longer, more expensive and obsolete.

EMS 4.0 Workflow: Improved decision-making, faster time-to-market, cheaper and with better quality. Lean design, Test and Manufacturing deliver Defect-Free products at lower cost!
ASTER Software Suite is articulated on two principles:

1. Simulate the manufacturing flow, from schematic or layout data, in order to identify the possible consequences of inadequate testability and test coverage, on a new design.
   - TestWay is the world leader in Test Coverage Analysis.
   - TestWay is delivering a digital twin for all test techniques: AOI, SPI, AXI, ICT, FPT, BST, FCT…

2. Qualify the customer defect universe using traceability and repair loops (big data analysis). This universe includes not only manufacturing defects, but also design and functional defects.
“What-if” Analysis

TestWay simulates the mixed test line:
- Estimate combined test coverage.
- Minimize test technique drawbacks such as:
  - number of test points,
  - test time,
  - false alarms,
  - diagnostic inaccuracy...

Functional test coverage (FT) estimations can be used in conjunction with complementary test strategies to provide total fault coverage i.e. AOI, AXI, ICT, FPT and BST.

EMS 4.0
- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion

If there is no solution, there is no problem
Enhanced Manufacturing Services 4.0

Close the loop - ASTER has designed a complete digital software suite including TestWay and QUAD: TestWay flow for Design to Delivery and QUAD traceability for continuous DfX feedback. Read more...
If there is no solution, there is no problem.

Good Products

- Good products must be defect-free at minimum cost.
- How to detect or prevent all faults on the product so that only good products are shipped?
- Is a board good because it passes the test?
- Test coverage is a key metric as it will be the quality warranty and the main driving factor for LeanTest.
Test Coverage

- Each test stage catches a subset of the defects.
- Overlapping tests have little or no value.
- Lack of test coverage results in faulty products shipped to the end-customer.

EMS 4.0

- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion
In order to consider all defects, including design validation and testing, we need 3 main defect classes:

- Design Defects
- Manufacturing Defects
- Functional Defects
Why do the layout before the DfT?
- Layout: End of the design!
- Design For Test: better design… for test purposes.
  = After the layout, it is always too late!
Design and Testability rules violations limit test coverage.

Accessibility requirements are back annotated, prior to layout, ensuring that the required physical accesses will be available where they are mandatory.
Placing probe ≠ DfT

- Test Point Optimization for real estate saving on high density boards.
- Test line balancing (avoid test shortfall, reduce test/inspection overlap), generate optimized test program.
- Maximize test coverage, minimize cost.

= Save money
The copper area having the required properties will be used as access points for In-Circuit Test or Flying Probe Test.

- Coverage
- Schematic Capture
- Electrical view
- Layout
- Physical view
- Physical access for test
- TestWay
- Mechanical DfT
- TestWay
- EMS 4.0
- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion

If there is no solution, there is no problem
If there is no solution, there is no problem

EMS 4.0
• Industry 4.0
• Good products
• Defect Universe
• Design Defects
• Manufacturing Defects
• Test Coverage
• Test efficiency
• Faulty boards
• Understand defects
• DPMO extraction
• Conclusion

Layout – Mechanical DfT

Electrical View
including test point requirements

Physical view

Schematic Capture

Layout

TestWay

Required Test points

Optimized physical Test Points & Test programs

Check the required test accesses versus real test point locations.

Test coverage report
We can improve only what we can measure.

- Reference point from early coverage estimation.
- Comparison point with real test program running on the shop floor.
  - Identify deviation, drive continuous improvement.
Test Coverage Measurement

More than 60 coverage importers

Acculogic (BS, Scorpion, SPRINT), Aeroflex (IFR4200, IFR5800), KeySight (SJ10, SJ50, 5DX, x6000, i1000, i3070, x1149), ASSET, CableTest, Checksum, CIRRIS, CKT, CORELIS, CyberOptics, DrEschke, ElovWert, EuroPlacer, GEDIS, GOEPEL (CASCON, OPTICON, XLINE), JTAG Tech, KohYoung, Matrix, MIRTEC, MODUS, MVP, MYDATA, OMRON, Orbotech (TRION, S22, S36), PEMTRON, Phoenix|Xray, SAKI (BF-Tristar, BF-Frontier, BF-X2), SEICA, SPEA (3030, 4040), SYNOR, TAKAYA (APT800, APT8000, APT9000, APT1400), TERADYNE (GR228x, TS124, Spectrum, Z1800), TRI (TR518, TR5001, TR7500, TR7600, TR8001), VISCOM, ViTechnology, ViTrox (V510, V810), WIZE, XJTAG, Yamaha, YESTech
Typical manufacturing defects:

- Missing components
- Misalignment
- Wrong value
- Incorrect Polarity
- Open Circuits
- Broken components
- Tombstone
- Short circuits
- Insufficient solder

We need to group defects into categories, to understand what defects can be captured by any particular test strategy.
Demonstration using an absurd example

✓ Board - 4 components: 3 resistors, 1 BGA.
✓ The 3 resistors are measured with very high accuracy.
✓ No test on the BGA.

✓ Is the board test score really 75%?
  3 resistors / 4 components

✓ We need something to weight the coverage…
  It must be credible, easy to update to reflect growing electronics complexity.
The ability to detect defects defined with a number: Coverage.

Each defect category fits within its test coverage:

<table>
<thead>
<tr>
<th>MPSF</th>
<th>PPVSF</th>
<th>PCOLA/SOQ /FAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material</td>
<td>Value</td>
<td>Correct</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Live</td>
</tr>
<tr>
<td>Placement</td>
<td>Presence</td>
<td>Presence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Alignment</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Orientation</td>
</tr>
<tr>
<td>Solder</td>
<td>Solder</td>
<td>Short</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Quality</td>
</tr>
<tr>
<td>Function</td>
<td>Function</td>
<td>Feature</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At-Speed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Measure</td>
</tr>
</tbody>
</table>
Test coverage by defect category

 каждой тестовой технике присуща определенная способность распознавать часть дефектного пространства.

 Нет одной единственной методики, которая может обнаружить все дефекты.

 Хорошая покрытие = комбинация тестов!

 Good coverage = combination of tests!
Test coverage by defect category

- For each category (Material, Placement, Solder) of defects (D), we associate the corresponding coverage (C).

\[
\text{Effectiveness} = \frac{\sum D_M \times C_M + \sum D_P \times C_P + \sum D_S \times C_S + \sum D_F \times C_F}{\sum D_M + \sum D_P + \sum D_S + \sum D_F}
\]

- The test efficiency is based on a coverage balanced by the defect opportunities.

We need a better coverage where there are more defect opportunities!
If there is no solution, there is no problem

Test coverage by defect category

If the board is failing at system test, it is usually because the escape rate (or slip) is higher than expected.

- There are only two possibilities:
  - The combined coverage is lower than optimal.
  - The DPMO figures are higher than expected.

Products shipped
- FPY
  - Good
  - Bad

Products repaired
- FOR
  - Good
  - Bad

EMS 4.0
- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion
Faulty boards at system level

The auditing conclusions were:

- Wrong or inadequate coverage metrics are produced: Example: confusion between accessibility and testability; coverage by component only - without incorporating solder joint figures; Over optimistic report (marketing driven report),
- Wrong DPMO figures, due to limited traceability or incorrect root cause analysis (Example: confusion between fault message and root cause/defect).

Selected strategies

- EMS 4.0
- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion
Understand defects

Test strategy and defect occurrence should be tied together.

- Strong test coverage on defects that occur frequently.
- Lack of coverage on defects that never occur has no consequence on the final quality.

= Qualify your test strategy against your real DPMO.
DPMO Extraction

❖ Current trend
  ✓ The historical web site sharing average DPMO in electronics industry has been closed.
  ✓ Case studies are 10 years old and no longer reflect modern production.

❖ ASTER Innovation
  ✓ Extract the true Defect Per Million Opportunities from the traceability database, built from your production line.
  ✓ Close the loop by using the DPMO to drive future test coverage estimation from schematic or layout.

EMS 4.0
• Industry 4.0
• Good products
• Defect Universe
• Design Defects
• Manufacturing Defects
• Test Coverage
• Test efficiency
• Faulty boards
• Understand defects
• DPMO extraction
• Conclusion
EMS 4.0
• Industry 4.0
• Good products
• Defect Universe
• Design Defects
• Manufacturing Defects
• Test Coverage
• Test efficiency
• Faulty boards
• Understand defects
• DPMO extraction
• Conclusion

If there is no solution, there is no problem
QuadDPMO case study

Test Coverage with standard DPM

Test Coverage with real DPM

Concentrate your test & inspection where defects really occur!
The Defect Universe, highlights that the majority of defects are due to manufacturing processes. In a double reflow soldering process, the “Open” category is the main contributor. The solder paste is reduced as much as possible to avoid micro-balls of solder rolling on the bare board causing “Short” defects, whereas insufficient solder is prone to create “Open” defects.
QuadDPMO case study

AOI and AXI: Most of the pure manufacturing defects (presence, alignment, short, open)

ICT/FPT and Boundary test (JTAG): at-speed defects, short between nets, component validation

Functional test: almost exclusively live defects
# Software Platform for Industry 4.0

## Traceability, Fault Diagnostic, Manufacturing Analytics

<table>
<thead>
<tr>
<th>Open Ecosystem</th>
<th>Advanced Viewing Solutions</th>
<th>3rd Party Software Integrators and Hardware Integrators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Support for over 60+ types of Assembly, AOI, AXI, ICT, FPT, BST &amp; Wiring test machines</td>
<td>Cross-probing Navigation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fault-ticket Analyzer</td>
<td>Plug-in 3rd Party SW</td>
</tr>
<tr>
<td></td>
<td>Test Coverage Analyzer &amp; Simulator</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Design for Test</td>
<td>Predictive Test Coverage</td>
</tr>
<tr>
<td></td>
<td>Test Strategy Simulation</td>
<td>Test Program Automation</td>
</tr>
<tr>
<td></td>
<td>Real Coverage Measurement</td>
<td>Test Report Automation</td>
</tr>
</tbody>
</table>

## Industry 4.0
- Industry 4.0
- Good products
- Defect Universe
- Design Defects
- Manufacturing Defects
- Test Coverage
- Test efficiency
- Faulty boards
- Understand defects
- DPMO extraction
- Conclusion

## EMS 4.0

- Support & Services

---

If there is no solution, there is no problem
Conclusion

❖ From design, during production and in a more general way, through the whole life cycle, coverage estimation permits the test process to be optimized.

❖ By deploying various testers in the best order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels raised.

❖ Gathering data from the test floor for analysis, and understanding failure data can help increase coverage.

❖ The economic challenges are critical: the tools to meet them are available.
ASTER Technologies
PO Box 7163
Colorado Springs, CO 80933-7163

Contact: William E. Webb
Tel: +1 (719) 331-0346
E-mail: sales-USA@aster-technologies.com
Web: www.aster-technologies.com