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Testability Guidelines

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SMTA TESTABILITY GUIDELINES
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FORWARD
Design for Testability and the SMTA Testability Committee

Just about one year ago, I was asked if I could update the SMTA Testability Guidelines, document TP-101B, that was published by the Surface Mount Technology Association (SMTA) in 2000. At first the task appeared simple. Because I found a few typos, I felt I could make a contribution by correcting them. With the typos corrected I reread the guidelines and had a nagging feeling that more was needed. The guidelines were all useful, but I knew that designers of circuits in 2002 and beyond needed guidelines to deal with technologies that were not in place at the time of the last writing.

Circuit complexity has increased tremendously in the short two-year span since the last guidelines were published. I suspected that there would be substantial changes and I needed help from professionals in various aspects of testability. Despite my foresight, even I did not realize how extensive the changes would become. While the 2000 version would be complete with one or two guidelines on such issues as Boundary-Scan, Vectorless Testing, Automatic Optical Inspection, Built-In Self Test, Analog and Mixed Signal, it became evident that several guidelines in each of these areas were needed, thus requiring subcommittees of experts. With support from the SMTA administration and members, as well as testability experts at-large, we were able to organize Task Forces dealing with each of these issues. Each Task Force was headed by a Task Force leader and was assisted by dedicated professionals who brought together these guidelines.

Throughout the year we had our trials and tribulations. With our own jobs and lives competing for priority, it was difficult to meet deadlines and to stay on course. Had it not been for the dedication and professionalism of all who were involved, we would not have been able to produce such a comprehensive set of guidelines. For my part, it was relatively easy to get results because the members pressed themselves to meet milestones.

No one in the committee was paid, but the reward we seek is the knowledge that we have helped our profession by making it possible to comprehensively test and accurately diagnose the complex circuitry produced - at least for the next few years. Unfortunately, we cannot rest on our achievements, for we know quite well that the future of electronics will make testing even more complex. In time, we hope there will be another group of dedicated professionals who will take on this task and come up with testability solutions for those circuits as well. They will tackle tougher problems and come up with better solutions, but the members of the 2002 SMTA Testability Committee who made this document possible will always stand out as true pioneers. With my greatest appreciation, I would like to now list them in alphabetical order, with bold letters designating Task Force Leaders:

Gerry Adams, Dade Behring
Jim Arient, Test Coach Corporation
Jinwen Chen, Huawei Technologies
Luciano Cornelio, Teradyne
Ray Dellecker, JTAG Technologies
Michael Early, Teradyne
Josh Ferry, Teradyne/ATE Ops
Chris Jacobsen, Agilent Technologies
Brad Jolly, Agilent Technologies
Jesse Katzman of SMTA
Michael Keller, American Society of Test Engineers
Joe Kirschling, Agilent Technologies
Jana Knezovich, Agilent Technologies
Glen Leinbach, Agilent Technologies
John McDermid, Agilent Technologies
Guoqing Li, Huawei Technologies
John Maxwell, JM Inc.

Carlos O'Farrill, Jabil Circuit
Barry Odbert, Agilent Technologies
Stig Oresjo, Agilent Technologies
Kenneth Parker, Agilent Technologies
David Rager, Design Solutions
Bob Stasonis, Teradyne
Robert Twigg, JTAG Technologies
Louis Y. Ungar, A.T.E. Solutions
Amit Verma, Teradyne
Don Walsh, Jabil Circuit
Keith Wainionpaa, Mesabi Electronics
Liz Weese, Jabil Circuit
Klaus-Jurgen Wolter, Technische Universitat Dresden
Zafei Yan, Huawei Technologies
Patrick Zarrabi, Harman OEM Group

We also want to thank those who constructed previous releases of this document. In many cases we have kept their guidelines intact. These individuals were an integral part of our group and their contributions should also be recognized.

In addition to these professionals, others have also contributed. Our work was recognized and encouraged by SMTA president Mr. Rod Howell of Libra Industries and by Mr. Michael Keller of the American Society of Test Engineers (ASTE). Mrs. JoAnn Stromberg has been encouraging this effort for many years, and it was due to her leadership and foresight that these Testability Guidelines are available to the electronics industry. Though already listed as an integral member of the SMTA Testability Committee, special thanks are due to SMTA director of publications Mr. Jesse Katzman, who kept us organized and who took the raw engineering writings we produced and made them fit well in a readable document.

There are many others to thank - managers, wives, husbands, and children - who gave up these members' "free time" so they could contribute to the profession. We hope you find that these guidelines are a great deal more valuable than the low price at which the SMTA is making them available.

Louis Y. Ungar
2002 Chair, Design for Testability Committee
Surface Mount Technology Association
September 2002

INTRODUCTION
An Overview of the SMTA Testability Guidelines

These Testability Guidelines were developed by various Task Forces, each concentrating on its own discipline. We present the work of the various Task Forces as separate chapters.

A general format applies to each task force and it was intended to assist the reader in dealing with the myriad of testability considerations that need to go into the design, development, and test of a product. The format we adopted was one used in previous SMTA Testability Guidelines. Each of the following chapters, dealing with the work of individual Task Forces, begins with an introduction and overview describing the subject matter the Task Force considered. Some of this is tutorial for those who need it, but it also provides valuable information to those who may be familiar with the subject of the chapter. It is intended to put into perspective the enumerated guidelines that follow. The guidelines are generally numbered, but there is no specific sequence intended.

Each bold-lettered guideline is usually followed by one or more paragraphs explaining or qualifying the guideline.

The Probing and Fixturing Task Force, with Jim Arient of Test Coach Corporation as the Task Force leader, developed Chapter 1, Probing and Fixturing Guidelines. These guidelines begin with considerations for tooling holes, datum point dimensions, probe pad sizes, and test via drill sizes. Guidelines follow on where probing should be performed, how probing points should be placed around tall components and near board edges. Test pad targets need also be properly planned in terms of solder coating, and guidelines are provided on what points should or should not be probed. Guidelines are given on head style probes to use for various contacts and how the probes should be distributed on the board. Some guidelines are also provided on minimizing the changes that will be required in the fixture when design changes occur.

Chapter 1 also provides a separate section for Flying Probe Guidelines. This section provides a formula for calculating the "Keep-Out Area" and guidelines on optimizing flying probe test times.

Luciano Cornelio of Teradyne headed the Vectorless Test and Fixturing Task Force. Its work is included in Chapter 2. The chapter begins with a clear description of how vectorless testing works. The guidelines start by advising against using vectorless testing with tape automated bonding (TAB) devices or with devices that have a ground plane above the device's lead frame. It also cautions using vectorless testing with boards containing heatsinks, tall components, ceramic stadium BGAs, and recommends adding labels after the in-circuit test. It contains some guidelines on the type of connectors to use on the board, and it recommends placing devices on the opposite side of the board if they create problems for vectorless testing. Some guidelines are offered to deal with polarized capacitors and through-hole devices as well. A number of guidelines are offered about building test fixtures that will be used in conjunction with vectorless test.

Mike Early of Teradyne led the Automatic Optical Inspection (AOI) Task Force, whose work is documented in Chapter 3. The group maintained that these guidelines be called "inspectability", rather than "testability" guidelines. The guidelines request unobstructed areas around the parameter of devices. They also guide on placement of markings and shading of areas around device

leads. Guidelines include placement fiducials information in the computer-aided design (CAD). There are restrictions on shared pads between components and split pads on a single component. Guidelines exist on marking pin 1 of integrated circuits (ICs), and on polarities of tantalum capacitors. Areas are to be reserved for conveyer belt clamping. Use of bar coding is encouraged.

The X-ray Task Force was led by Amit Verma of Teradyne, and its work is contained in Chapter 4. A distinction is made between manual X-ray inspection (MXI) and automated X-ray inspection (AXI), which requires no operator intervention. There is also a distinction between a 2-dimensional X-ray, called a transmission AXI, and a 3-dimensional X-ray, called cross-section AXI. First, there are six guidelines that apply to all X-ray methods. They include considerations for board rigidity, and uniform size for pin 1. A guideline is provided for transmission AXI to minimize overlapping solder joints on double-sided boards. A guideline for cross-section AXI requires surface map locations for laminogrpahic systems.

Chapter 5 is the work of the Electrical Design Task Force. It is the largest section that has been added to the work previously included in the earlier SMTA Testability Guidelines. Gerry Adams of Dade Behring led this task force to publish the 30-or-so guidelines that cover a variety of applications, including, in-circuit test, functional board test, and analog test. Many of the guidelines are methods traditionally used to gain controllability and observability of circuit nodes. Some of the guidelines are new. Others are revised. For example, a table is included that provides guidelines on the resistance values for pull-up resistors for various logic families and for various supply voltages. This chapter contains general testability guidelines and includes all those that could not be directly attributed to a specialized Task Force.

The Boundary-Scan Task Force, led by Ray Dellecker of JTAG Technologies, produced Chapter 6. In the previous edition of the SMTA Testability Guidelines, the IEEE-1149.1 was relatively new, and nearly the only relevant guideline was to encourage people to use it. In the past two years, however, boundary-scan has seen a tremendous growth, mainly because it is the only practical way to access BGA devices. Also, programmable devices, such as CPLDs and FPGAs, have adopted the boundary-scan port (also called the JTAG port) as the de facto standard access to program these devices. With boundary-scan offering access without the need for bed-of-nails or flying probe, it has become a flexible element in most test strategies. Chapter 6 discusses the uses of boundary-scan extensively before it offers specific guidelines.

The guidelines themselves are categorized in the following groupings:

- Device selection and documentation
- General board design rules
- Test access port (TAP) signals
- In-system programming considerations
- Design practices
- Access to the target board

Within each of these categories there are suggestions on how to optimize the benefits that one can gain from the use of boundary-scan. The importance of these guidelines are coming to light as more and more ICs come out of foundries with boundary-scan as a standard rather than an optional feature. Many board designers are finding their boards testable (with boundary-scan) often without even trying.

Kenneth Parker of Agilent was drafted to lead the Analog & Mixed Signal Task Force. Discussions about what to include resulted in an agreement to limit the work of this task force and the scope of Chapter 7 to the IEEE-1149.4 standard. A short discussion of the standard is included as a tutorial, since at the time of this writing 1149.4 is sparsely used. Like its digital predecessor, the IEEE-1149.1 is slow to be accepted but is likely to pick up quickly. Thus we felt that it was appropriate to provide some guidelines here. The guidelines deal with the use and connection of 1149.4 components at the board level.

Chapter 8 is the work of the Built-In Self-Test (BIST) Task Force, led by Louis Y. Ungar of A.T.E. Solutions, Inc. A brief tutorial on BIST demonstrates how chip-level, board-level, and system-level BIST structures can be built and integrated in a hierarchical manner to become part of the overall test strategy. The guidelines encourage the use of devices equipped with BIST and boundary-scan and the use of both of these mechanisms to assist board-level BIST. Diagnostic capabilities of BIST are stressed, and the building block approach of testing the built-in tester before it tests the rest of the circuit is encouraged. Some guidelines are also offered on software and firmware built-in test (BIT). Guidelines are provided to reduce the reliability impact of additional circuit for BIST, as well as for filtering of false alarms.

Finally, a glossary is provided for terminology used in these guidelines, as well as in testing in general, and a reference section is included for further research.

The effort of revising the 2000 SMTA Testability Guidelines proved that a great deal has changed in just two years. Undoubtedly, readers will find new issues that were not addressed.

User comments on these guidelines are solicited. All responses should be addressed to the SMTA Testability Committee: 5200 Willson Road, Suite 215, Edina, MN 55424 - P. 952-920-7682, F. 952-926-1819, E. smta@smta.org

CHAPTER 1
Probing and Fixturing Guidelines

Probing guidelines are needed when bed-of-nails contact is anticipated. Automatic test equipment (ATE), such as in-circuit (ICT), connectivity and manufacturing defect analyzers (MDAs), depend on making reliable contacts with certain circuit nodes. These guidelines are intended to increase the number of possible contacts as well as the reliability of those contacts at a feasible cost.

Test Points

The term test point, as used in this section, refers to any feature that is probed during electrical test, such as test via, test pad, and through-hole lead.

A test via is a plated through-hole with an exposed annular ring; the test probe strikes either the solder that fills via holes during processing or the outer edges of the empty via barrel.

A test pad is a solid area of exposed metallization; there is no through hole; the test probe strikes the flat surface of the feature.

All test points should be identified properly as a test point and associated with a net in the PC board's database in computer aided design (CAD) or on the schematic. In CAD, if a surface pad is placed and connected with a trace to a component pin but not logically connected in the PC board database, it may be missed and not assigned a test probe in the test fixture.

Tolerances

The criteria used in the tolerance analyses consisted of:

- a single point (spear head) probe,
- the worst-case tolerance internal to the probes and their mounting,
- tolerances associated with unit under test (UUT) platen (probe plate) alignment, and
- test pad diameter.

Statistical analysis of the number of contact misses was not considered, since a contact failure on any test caused by improper tolerancing is not acceptable and invalidates the test.

With larger PC boards, these tolerances become more difficult to control than with smaller boards. The tolerance build-up directly and adversely impacts test pad size. As the board size increases, larger diameter test pads may be required in order to maintain probe contact reliability.

Flying probe fixturing guidelines are discussed separately in a section of their own at the end of this chapter with guideline numbers starting #FP-1. General guidelines that typically apply to bed-of-nails fixtures are discussed first and start with #P-1.

A flying probe tester can perform many of the same tests that ICT using bed-of-nails fixturing provides. The flying probe tester is a fixtureless tester that utilizes several moving arms with test probes to access all test points on a PC board. Typically, the PC board is placed upside down in the tester, and multiple arms with test probes move across the bottom side of the board, touching down on test points and taking measurements. The biggest advantage of this test is that it does not usually require a test fixture. It's greatest limitation is that it has long test times due to the arm movements.

CHAPTER 2
Vectorless Test and Fixturing Guidelines

In some cases devices may be tested using vectorless test techniques. These devices are generally:

- complex digital devices where library tests either do not exist or would take a long time to create,
- connectors using in-circuit test (ICT) methods to test for solder opens, and
- polarized capacitors using ICT methods to check for proper polarity.

When a board includes any of these devices, this section describes appropriate design for test (DFT) guidelines. Vectorless tests check device pins for open solder joints without testing the device core logic (or IC die). These tests use analog measurements to check the solder joints. Since core logic is not tested, these tests do not require any library device test and can be executed on digital, analog, or mixed signal devices.

The basic vectorless test procedure applies a low voltage sine wave to a device pin-under-test (see Figure VT-1). The test also ties all other (accessible) pins on that device to system ground. The source voltage's load becomes the cumulative capacitance between the pin-under-test's lead frame and the lead frames of all other device pins (Cig). A vectorless test sensor plate above the device-under-test receives a test voltage through the capacitive coupling between the device lead frame and the sensor plate (Cvt).

A test system digital volt meter (DVM) measures this voltage. The amount of voltage at the sensor plate varies with the Cvt impedance. If a sensor plate amplifier is used, a typical Cvt value (50-100 fF) couples sufficient sensor plate voltage for a repeatable vectorless test. If the pin-under-test is open, the open forms a small capacitance between the pin and the PC board pad. This produces the signal in Figure VT-2.

This open capacitance (Copen) forms a voltage divider with Cig. This greatly reduces the voltage applied to the pin-under-test's lead frame, also reducing the measured sensor plate's voltage. A typical IC open reduces the lead frame voltage by 1 to 2 orders of magnitude from the input voltage, facilitating open pin detection.

With some modifications, this basic technique tests ICs, connectors, and polarized capacitors. To check capacitor polarity with this technique, the test adds very precise low impedance analog measurements across the capacitor.

An alternate vectorless test technique can be used to test ICs. This technique applies and measures test signals through IC substrate diodes and parasitic resistances. This does not use the capacitive coupling between device lead frames and vectorless test sensor plates. This test, however, is less stable, with results that vary with the IC type and die. The DFT guidelines for this section concentrate on the more stable sensor plate measurement vectorless test method.

CHAPTER 3
Automated Optical Inspection (AOI) Guidelines

These guidelines are an overview applicable to the majority of AOI equipment available on the market today. There are limitations to the scope of these guideline, though. Certain advanced detection capabilities and their DFI requirements are not discussed here, due to their specialized nature and application.

Background

In the high volume manufacture of printed circuit assemblies (PCAs) it is critically important to automate every step in the process in order to meet the desired overall production rate and quality levels. This includes completely automated inspection of the product. Automated optical inspection (AOI) is an enabling technology that delivers comprehensive inspection of a complex PCA at the full run rate of the production line.

The manufacture of a product is comprised of many steps. Case studies have shown that manufacturing stages can be optimized for speed and their cost reduced if the manufacturing stages are taken into consideration during the design phase. By today's standards, design for manufacturing is a requirement for successful, efficient production and reliable products.

In order to remain competitive, an increasing number of manufacturers have realized that designers must consider more than just design for manufacturing as it relates to product assembly. To keep costs low and quality high, design for testability and inspectability has now gained wide acceptance.

Automated optical inspection technology is now being deployed widely and has many benefits:
· Automated systems are orders of magnitude faster than human inspectors.
· AOI systems are vastly more accurate and objective than human inspectors.
· AOI systems make repeatable, stable judgments.

Consistent with design for testability, design for inspectability can greatly improve the efficiency of the manufacturing operation and the quality of the resulting products.

It is useful to identify inspectability issues and create guidelines for incorporation into the design cycle. This document identifies most of the standard inspection issues, and suggests guidelines that will result in maximized defect detection at the AOI process step.

The current generation of AOI systems has a fairly well defined set of fault detection capabilities. The commonly employed fault detection types that leading AOI systems can deliver include:
· Placement faults (missing, skewed, tombstone, billboarded, etc.)
· Solder faults (no, low, excess, bridging)
· Other (lifted lead, bent lead, wrong component, etc.)

The techniques that are employed to achieve these inspections depend on having visual access to the areas of interest, and they also depend on certain visual attributes to make good vs. bad judgments. If visual access is blocked, or if the visual attributes of the PCA are not consistent with the requirements of the AOI techniques, fault coverage is degraded.

To ensure high fault coverage at the AOI process step, the design group can elect to follow a set of design for inspection (DFI) guidelines that will maximize fault detection in manufacturing. Following these guidelines can result in higher product quality, more efficient manufacturing, and reduction of missed faults (escapes) reaching the customer.

The reader can gain the following from this chapter:

- An understanding of the basic inspection techniques employed by an AOI system.
- An understanding of some of the visual attributes of a PCA required for reliable fault detection sing AOI.
- A list of general design practices for maximizing the inspectability of a printed circuit assembly.

CHAPTER 4
X-ray Inspection Guidelines

Definition and Discussion of Terms

Manual X-ray Inspection (MXI) and Automated X-ray Inspection (AXI)

X-ray inspection systems are available in both manual (MXI) and automated (AXI) varieties. MXI systems can have varying degrees of automation and can include varying degrees of automated board handling and image processing functions. What generally distinguishes AXI systems from MXI systems is that AXI systems are in-line capable and do not require the help of an operator to make pass/fail decisions.

MXI equipment is almost exclusively transmission X-ray technology, whereas AXI equipment can be transmission, cross-section or combo (see below).

Transmission, Cross-section and Combo AXI

AXI equipment is generally available in three forms:

- Transmission AXI - commonly referred to as "2D" X-ray
- Cross-section AXI - commonly referred to as "3D" X-ray
- Combo AXI

Transmission AXI automatically generates images of all features between the X-ray source and the detector. Cross-section AXI automatically generates images of one horizontal slice of the board at a time, usually a minimum of one slice on each of the board's top and bottom sides. Laminography and digital tomosynthesis are the most common implementations of cross-section AXI.

Combo AXI equipment uses a combination of transmission and cross-section techniques concurrently during the inspection of a printed circuit board (PCB). Combo systems automatically apply each technique where it is best suited and allow users the ability to select one technique over another if desired.

Transmission, cross-section, and combo X-ray techniques are all capable of detecting PCB assembly defects that cause changes in the solder joint profile. These types of assembly defects include, but are not limited to, solder shorts, solder opens, solder voids, insufficient solder joints, missing devices and skewed devices.

On double sided boards, some subset of the solder joints will be inaccessible to the transmission X-ray technique due to overlap, whereas the cross-section technique will have greater test access. Because the transmission X-ray technique captures information from the entire solder volume and the cross-section technique captures specific "slice" information, these techniques have both unique and common capabilities to detect some types of solder defects. For more detailed information, contact the manufacturers of AXI systems who can provide information about the capabilities of their techniques and systems.

CHAPTER 5
Electrical Design Guidelines

In addition to specific testability guidelines discussed in other chapters, the Electrical Design Guidelines serve as a general design for testability approach. The 30-or-so guidelines that follow cover a variety of applications, including, in-circuit test, functional board test, and analog test.

Many of the guidelines are methods traditionally used to gain controllability and observability of circuit nodes. Some of the guidelines are new. Others are revised. For example, a table is included that provides guidelines on the resistance values for pull-up resistors for various logic families and for various supply voltages.

This chapter contains general testability guidelines and includes all those that could not be directly attributed to a specialized Task Force.

CHAPTER 6
Boundary-scan Design Guidelines

Purpose of This Document and Background of IEEE Std. 1149.1

When it became apparent that electrical access to complex circuit boards would become increasingly difficult, a group of interested manufacturers proposed a means of serial access over a small number of wires or contact points. Out of this work grew the Joint Test Action Group (JTAG), which later became a working group of the IEEE, chartered to develop the idea into a standard. The results of their work are defined in the IEEE Std. 1149.1, *Test Access Port and Boundary-scan Architecture*, often referred to as the JTAG standard. Similarly, the IEEE-1149.1 Test Access Port is often called the "JTAG port." To complicate matters, the JTAG port is often used to program certain programmable devices, and in such cases boundary-scan may not even exist within the device. In this chapter we will use the terms "IEEE-1149.1" and "JTAG" interchangeably and, unless we state otherwise, we assume that boundary-scan is part of the circuit.

The IEEE-1149.1 standard defines a four-wire serial interface (a fifth wire is optional) to access complex digital integrated circuits (ICs), such as microprocessors, DSPs, ASICs, and CPLDs. To be compatible with the standard, the IC must contain a number of registers and a state machine (the TAP controller) to execute the boundary-scan functions. Depending on the state of the TAP controller, data enters the chip on the TDI pin, is stored in one of the data registers or the instruction register, and shifted out from the chip on the TDO pin. The boundary-scan logic is clocked by TCK, independent of the system clock. The TMS signal controls the state changes of the TAP controller.

In normal operation, a scan-compatible IC performs its intended function as though the boundary-scan circuits were not present. However, when testing or in-system programming is to be performed, the device's scan logic is activated. Data can then be sent to the IC and read from it using the serial interface. This data may be used to stimulate the device core, drive signals outward from or to the PCB, sense the input pins from the PCB, or sense the device outputs.

The scan modes of operation provide the ability of boundary-scan to test a board for structural faults that can occur during manufacturing and to perform in-system device programming - all via the standard JTAG test access port.

Multiple scan-compatible ICs may be serially interconnected on the printed circuit board, forming the boundary-scan chain, and a board may contain more than one scan chain. The scan chain provides electrical access from the serial TAP interface to every pin on every IC that is part of the chain. The result is that each boundary-scan cell becomes a virtual test point, significantly reducing the number of actual test points needed on the board.

To take advantage of the test capabilities of boundary-scan, it is mandatory that the unit under test (UUT) be designed properly in compliance with a number of device selection and control considerations. This chapter discusses the design for test (DFT) considerations beginning with a section on the use of boundary-scan in manufacturing applications. Following that, a review of Test Strategy Considerations and Integration Alternatives is presented. Then, the details of boundary-scan DFT and in-system programming design guidelines are covered.

CHAPTER 7
Analog and Mixed Signal Guidelines

The chapter on Electrical Design contains a number of general analog and mixed signal testability guidelines. This chapter concentrates on those that involve circuits that comply to the IEEE-1149.4 standard.

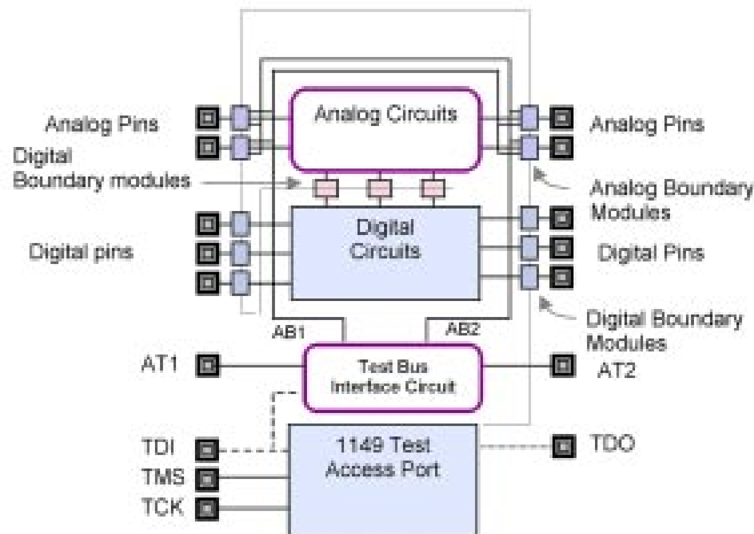

Figure 1149.4-1: IEEE-1149.4 mixed signal test bus.

The IEEE-1149.4 standard is an extension of the IEEE-1149.1 standard and consists of additional structures added to a 1149.1-conformant component. The IEEE-1149.4 standard defines test features and associated protocols for testing opens and shorts among device interconnections; it is for making analog characterization measurements and for testing the presence and value of discrete components both between and within devices.

Test access is gained through the familiar test access port (TAP) and through additional analog busses AT1 and AT2. Stimulus is provided to the AT1 bus, and measurements are through the AT2 bus. The test bus interface circuit connects AT1 and AT2 to a pair of internal busses, AB1 and AB2, connecting to each analog boundary module. Instructions passed to the TAP controls how a pin is connected to the AB1 and AB2 busses and disconnected from the analog circuits within the device.

Within each analog boundary module, in addition to the switches that connect to the AB1 and AB2 busses, is the circuitry necessary to both drive and receive a logical level at a device pin. The protocols to drive and receive logical levels parallel the IEEE-1149.1 standard, allowing interconnect testing between both 1149.4 devices and 1149.1 devices.

The IEEE-1149.4 standard was originally conceived to address the problem of mixed-signal device testing. During the period between its conception and the present, digital parts have taken on some of the characteristics of mixed signal devices. In the quest for speed, digital interconnections have become networks. The IEEE-1149.4 standard is equally well suited to test strictly digital devices and their interconnection networks.

CHAPTER 8
Built-in Self-test Guidelines

Built-in self-test (BIST) has found its way into today's circuits and is no longer a theoretical dream.

Built-in test (BIT) provides the mechanism for applying test stimuli, collecting the test responses, and deciding whether to PASS or FAIL for each test. BIT in system-level applications, especially software-driven BIT, is quite mature and has been part of electronic systems for most of the past 50 years. The difference between BIT and BIST is often a subject of intellectual debates, but the most common qualification for BIST appears to be the ability to perform BIT without the need for external circuitry - thus the "S" for "self" test.

The BIST designation, however, does not guarantee that extra circuitry has not been added. If an integrated circuit (IC) contains a mechanism inside the device, the board and system test user may well call this mechanism BIST rather than BIT, because from his/her perspective the IC is testing itself, and the mechanism used is not transparent to the IC purchaser. For this reason, all IC-level BIT is called BIST, board-level BIT is sometimes called BIT and sometimes BIST, and system-level BIT usually is called BIT.

IC-level BIST mechanisms often utilize pseudorandom pattern generators and signature analyzers and create structures that either exhaustively or pseudo-exhaustively test a large portion of the IC. See Figure BIST-1 for a popular BIST scheme, called Built-in Logic Block Observer (BILBO). More and more complex ICs are being produced and sold by IC vendors, and control of the IC-level BIST can be readily executed during the RunBIST state of the boundary-scan finite state machine detailed in IEEE-1149.1 (see chapter on Boundary-Scan).

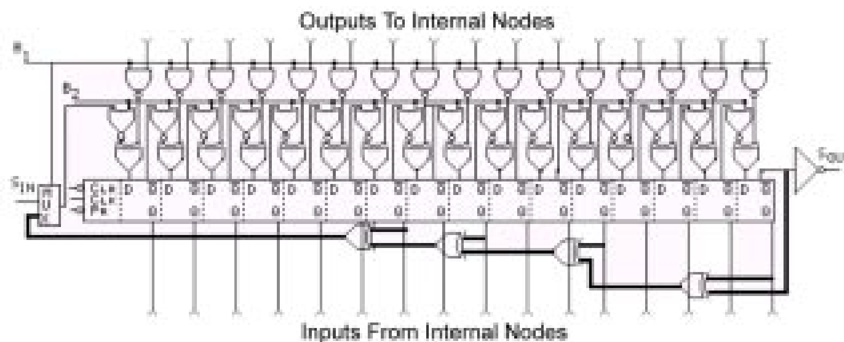

Figure BIST-1: An internal IC BIST scheme utilizing scan and signature analysis.

Several tools can be identified to assist in BIST at IC-, board-, and system-levels. These tools may be direct registers, scan registers (such as those used in boundary-scan or signature analyzers), and psuedo-random pattern generators. Figure BIST-2 and Figure BIST-3 show examples of BIST stimulus generating and BIST response collection tools, respectively.

Even when the IC is assembled on the board, IC-level BIST can be invoked and its results sent off the board for evaluation through the boundary-scan TDO line. In more recent applications, two BISTed ICs can be made to communicate with each other at real unit under test (UUT) speed, collect the responses in a boundary-scan register, and transport the result off the board using a lower speed TCK and TDO line.

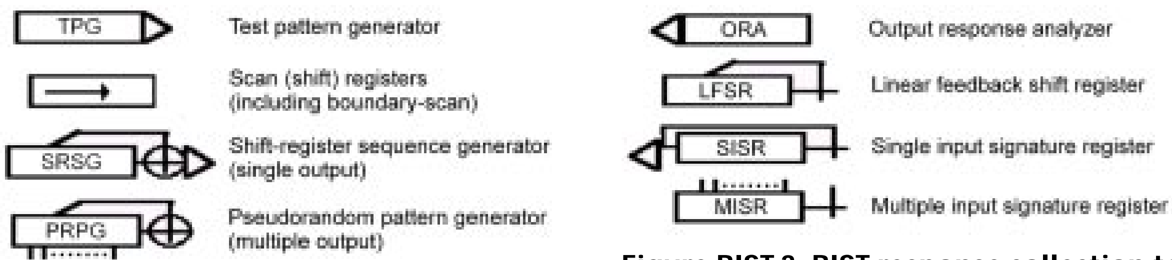

Figure BIST-2: BIST stimulus generating tools.

Figure BIST-3: BIST response collection tools.

With such applications, real-time board-level BIST is performed. Other board-level BIST techniques, though not necessarily at-speed, can also be performed. For example, some boundary-scan devices can reconfigure their boundary-scan ports so that they can apply pseudo-random test patterns to neighboring chips.

Similarly, test results can be compacted in signature analyzers and only the final results sent off the board. In other cases, chips are added to the board to facilitate board-level test. For example, a PROM can contain the stimuli and/or the expected results of a test, and a comparator can be used as an evaluator. In some cases there is little or no diagnosis beyond calling out the faulty board, but in many applications today board-level BIST can offer fault isolation to a single or to a few suspected components. Figure BIST-4 shows an example of a board-level BIST design.

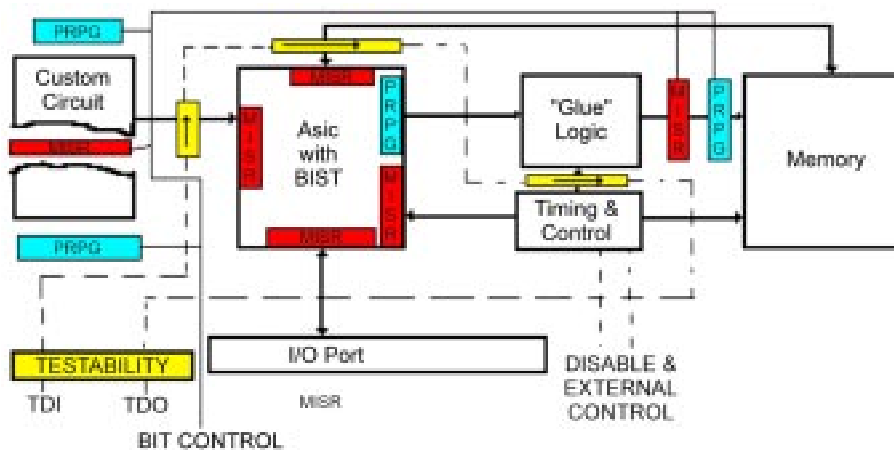

Figure BIST-4: Board-level BIST using BIST tools and boundary-scan.

At the system-level, BIT is primarily tasked with ensuring that proper flow of the functional cycle is maintained. Any deviations are to result in a system-level BIT failure. As in the case of board-level BIST, fault isolation is also needed for proper repair. The interaction of board-level BIST and its IC-level BISTs enables system-level BIT to identify with certainty the responsible board and component in many cases. This approach, called hierarchical BIST, is an achievable goal in many systems designed today. The reward is a sizeable reduction in the cost of test equipment and test program development, better product support, and the ability to find in-use problems.

A necessary ingredient for a BISTed circuit at the IC-, board-, and/or system-levels is design for testability. Some guidelines for improving BIST (BIT) testability at each of these levels are presented below.

GLOSSARY

In addition to the terms included below, we urge readers to visit a glossary maintained by *Test & Measurement World* on-line:
www.e-insite.net/tmworld/index.asp?layout=siteInfo&doc_id=76871

AOI - Automated optical inspection.

ATE - Automatic test equipment, a class of board testing equipment, which accesses the target via a set of test, probes (bed of nails).

BGA - Ball grid array, a chip-size packaging technique in which the electrical connections to the device are made by reflow solder balls on the bottom of the device, thereby eliminating the possibility of direct physical contact for electrical probing.

BIST - Built-in self-test, a test algorithm supported by the device itself, which can be activated by an IEEE-1149.1 instruction.

BSDL - Boundary-scan descriptive language, a file conforming to the format prescribed in 1149.1, which describes the boundary-scan implementation contained in a specific device.

(C)PLD - (Complex) programmable logic device, an IC that is in almost all cases programmable in-system via boundary-scan.

Defect Detection - Faults found and indicted as unacceptable by the AOI system.

DFI - Design for inspectability.

DFT - Design for testability, the process by which a system design takes into consideration the test coverage that can be achieved in production.

EIA - Electronic Industries Alliance.

Escape - A true defect that was undetected by the test or AOI system.

False Flag - An incorrect defect detection made by the AOI system.

Fault Class - Refers to the specific sub-types of faults that an AOI system can detect, such as missing components, skewed, tombstone, billboard, low solder, etc.

Fault Coverage - Refers to a group of fault classes that describe intended or resultant (actual measured) defect detection.

FPGA - Field-programmable gate arrays. Customizable logic arrays usually available in very large configurations and suitable for on-board programming.

Flash Memory - A non-volatile memory technology that can be programmed in-system.

IEEE-1149.1 - The boundary-scan standard, first published by the IEEE in 1990.

ICT - In Circuit Tester. A type of ATE where each component is tested after it is mounted on the board (as if it was not influenced by neighboring components).

ISP - In-system programming, the technique of programming devices after they have been soldered into the circuit board.

IPC - Association Connecting Electronic Industries.

JTAG - Joint Test Action Group, the ad-hoc industry committee that formulated the IEEE-1149.1 specification.

PCA - Printed circuit assembly.

PCB - Printed circuit board.

TAP - Test access port, the 4- or 5-wire interface to a boundary-scan device, consisting of the TDI, TDO, TMS, TCK, and (optionally) TRST* signals.

Test Pad - A solid area of exposed metallization; there is no through-hole; the test probe strikes the flat surface of the feature.

Test Point - Any feature that is probed during electrical test, such as test via, test pad, and through-hole lead.

Test Via - A plated through-hole with an exposed annular ring; the test probe strikes either the solder that fills via holes during processing or the the outer edges of the empty via barrel.

UUT - Unit Under Test. Whatever is being tested. Can refer to components, boards, modules or systems. In most cases in this document it refers to boards under test.

SMEMA - Surface Mount Equipment Manufacturers Association.

SMTA - Surface Mount Technology Association.

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IEEE Standard 1149.4-1999, *IEEE Standard for a Mixed Signal Test Bus*, New York, 1999.

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IEEE Standard for Embedded Core Test:
http://grouper.ieee.org/groups/1500/

IPC SM-782, *Surface Mount Design and Land Pattern Standard*.

IPC A-610C, *Acceptability of Printed Board Assemblies*.

NEXUS 5001 Forum:
http://www.ieee-isto.org/Nexus5001/about.html

SMEMA 3.1 *Fiducial Mark Standard*: This SMEMA standard is for fiducial marks. It facilitates the accurate placement of components on printed circuit boards.

Books and Tutorials

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Texas Instruments, SN74LVT8996 *Addressable Scan Port*:
http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=SN74LVT8996

National Semiconductor, SCANPSC100F *Embedded Boundary-Scan Controller*:
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http://www.e-insite.net/tmworld/
index.asp?layout=Community&industry=Design+for+Test+%2F+Built%2Din+Self%2DTest&industryid=19026

Boundary-scan tools are commercially available from the following companies (and perhaps others):
Acculogic - www.acculogic.com
ASSET Intertech - www.asset-intertech.com
Corelis - www.corelis.com
Flynn Systems - www.flynn.com
Goepel Electronics - www.goepel.com
Intellitech - www.intellitech.com
JTAG Technologies - www.jtag.com