

3D Packaging Applications, Requirements, Infrastructure and Technologies

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Course Scope

This course will take a broad and in depth view of the applications, technical through business requirements for the leading or emerging 3D packaging solutions and their associated supply chain infrastructures.

What you will learn:

This course will help you decide when and how 3D package integration can provide system or component benefits. How to evaluate and select the optimum 3D package technology based on the complex mix of cost, performance and business / logistic requirements. Where industry standards, device floor-planning and supply chain infrastructures; can reduce the total cost or time to market when implementing a 3D solution. How 3D platform technologies and industry roadmaps can be projected or shaped for next generation device integration to system design requirements.

A summary of the surface mount process parameters for PoP stacking both single pass reflow and pre-stacking.

A method will be introduced for rating and ranking the adoption risks for new package technologies or supply chains. This method can be used as a tool for new technology adoption, component procurement or product development requirements.

3D Package Technologies to be reviewed include:

MCP – multichip package, components using a combination of stacked, wire bonded memory die, also referred to as stacked die package or stacked CSP.

SiP = system in a package, uses a combination of stacked logic and memory die with wirebonding or a mix of FC and wirebond interconnects.

PoP = package on package, uses stacked packages where logic and memory components are produced separately and stacked in the OEM's surface mount assembly flow.

Embedded chip technologies where active or passive chips are embedded in printed wiring or thin film build up circuits with interconnect patterns on both sides.

Wafer level 3D packaging including die on wafer, wafer on wafer and TSV approaches.

TSV = thru silicon vias, where memory die are designed for thru Si via connection to enable multiple die to be stacked in a flip chip style assembly flow to increase memory capacity in the smallest / thinnest package profile.

A section of the course will review real world high volume 3D package technologies used in multimedia mobile handsets. Quantify the technical and business / logistic requirements and trends that make up the total cost of ownership equation.

The course will explore the critical role industry infrastructure and standards play in new 3D package platforms by summarizing the package on package collaboration efforts and results.

Take away benefits include:

- 3D package market forecasts by application and technology.
- A review of current and emerging 3D packaging technologies to understand their cost / performance, supply chain capabilities.
- JEDEC Standards and Infrastructure Development examples.
- SiP vs PoP Cost / Performance Comparisons.
- A quantitative method for rating and ranking the technical and logistical risks in adopting new packaging technologies or technology transitions.

Instructor Bio:

Lee is recognized as an industry expert in 3D packaging, with over 27 years of diverse technology and end market applications experience. Beginning in early 80's with flex circuit based folded or dynamic flex assemblies for hearing aids, hard disk drives, cameras, portable PC and automotive applications.

Over the past 10 years Lee held 3D packaging technology, infrastructure and business development responsibilities at Amkor, Texas Instruments and Tessera with market emphasis in mobile handsets.

Lee has authored or co-authored numerous patents, technical papers and industry articles. Authored the Stacked / 3D Packages chapter in McGraw-Hill's "Area Array Packaging Handbook."

Lee was responsible for definition, development and deployment of PoP technology while at TI. Successfully drove the co-development of PoP between Nokia, TI and Amkor, resulting in 15 month product launch from the final concept. The past few years Lee has been instrumental in the infrastructure development for PoP including JEDEC standard development, stacking process capabilities and board level reliability reports.

Lee's 3D packaging workshop at past IWLPC and SMTAI events were highly rated by attendees and conference organizers.